Union College
Union | Digital Works

Honors Theses | Student Work

6-2019

Designing a Low-Cost Ultrasound Pulser

Andrea Huey
Union College - Schenectady, NY

Follow this and additional works at: https://digitalworks.union.edu/theses

 Part of the Bioimaging and Biomedical Optics Commons, Electrical and Electronics Commons, and the Electronic Devices and Semiconductor Manufacturing Commons

Recommended Citation
Huey, Andrea, "Designing a Low-Cost Ultrasound Pulser" (2019). *Honors Theses*. 2304.
https://digitalworks.union.edu/theses/2304

This Open Access is brought to you for free and open access by the Student Work at Union | Digital Works. It has been accepted for inclusion in Honors Theses by an authorized administrator of Union | Digital Works. For more information, please contact digitalworks@union.edu.

Designing a Low-Cost Ultrasound Pulser

ECE-499: Capstone Design Report

By

Andrea Huey

Advisor: Professor Takashi Buma

* * * * * * * * * *

Submitted in Partial Fulfillment

of the requirements

for Honors in the Department of Electrical Engineering

UNION COLLEGE

June, 2019

SUMMARY/ABSTRACT

Ultrasound imaging allows for those studying living beings to see inside a subject without causing it harm. This allows for real-time images to be taken, leading to ease of observational research. However, while this technology is beneficial to those who utilize it, the devices used to create and receive ultrasound pulses can be incredibly complex, allowing for precise adjustment of the output signal and various other functions, and therefore expensive. The focus of this senior project is the design of a low-cost pulser for use with an ultrasound transducer. While it does not have all the high-level functions of the original device, it has the same base functionality, most obviously the ability to output a high voltage pulse. The final output signal of the device is of sufficient pulse depth and width to drive an ultrasound transducer. Because this project set out to create a practical, low-cost alternative to the industry device, one large secondary requirement was cost—the device was constructed using a limited budget. This report will discuss the background necessary to understand both ultrasound imaging and the components used, before moving into a justification of component choices and the preliminary proposed design. From there, modifications to the preliminary design made before the final device will be discussed, as well as some performance estimates and results. Lastly, the design implementation schedule will be examined, an analysis of the costs of the device will be performed, directions on using and troubleshooting the device will be provided, and conclusions and further recommendations will be made.

TABLE OF CONTENTS

TABLE OF FIGURES AND TABLES

1. INTRODUCTION

Ultrasound imaging is an incredibly powerful, useful technology. It allows for medical practitioners and those studying living beings to see inside a patient or subject without having to cut them open or otherwise harm them. This process allows for real-time images to be taken, making it easy for doctors to diagnose and researchers to find what they are attempting to observe. Ultrasound imaging works by using an ultrasound transducer to send a very high frequency sound wave into the thing being imaged, then measuring the return echo. If the sound wave encounters something within the object, it will reflect off that, not the back end of the object. By graphing these reflections, an image can eventually be formed. The most well-known form of ultrasound is fetal ultrasound, used for medical applications. These images are often created using an array of hundreds of transducers. In the case of this project, the device is meant to drive only one ultrasound transducer. This allows for very precise imaging, as it is much easier to control the single transducer. This kind of ultrasound can also be used for non-destructive testing, as the user would send an ultrasound pulse through a transducer and hopefully not read any cracks or breaks in the device being tested. However, while this level of accuracy in research and testing can be quite beneficial to those attempting to utilize it, the devices used to create and receive ultrasound pulses can be fairly complex, allowing for very precise, fine-tuned adjustment of the output signal, and therefore expensive. Although this degree of function is often desired, as it can produce better, higher quality images, it is not often necessary. Professor Buma currently owns a device for driving an ultrasound transducer that costs approximately $2,000. He is able to use it for his research, but sometimes he requires more than one ultrasound transducer for his research. At the price of the industry device, purchasing many would not be cost-efficient.

Though the manufactured device is very high-functioning, he sometimes does not require as high a degree of functionality as it can provide. An image of the industry device is shown below in Figure 1 [1].

Figure 1: Image of the Industry Device this Project is Attempting to Replicate

Therefore, the problem this project sets out to solve and a solution to said problem become obvious. This project is focused on designing a low-cost pulser/receiver for use with an ultrasound transducer. While it will not have all the high-level functions of the original device, it will have all of the base functionality, most obviously the ability to output a high voltage pulse and receive a low voltage input. Some input adjustments are also desired, such as the ability to change the repetition rate or trigger type. Because this project sets out to create a practical, low-cost alternative to the industry device, one large secondary requirement is cost—the project must be able to be constructed using a limited budget. Because Professor Buma could potentially require the use of more than one of these low-cost devices, the design should also be fairly easy to replicate. The design should also be fairly adaptable, so that components can be replaced with ease. This will allow for future improvements to be made upon the device.

Ultrasound pulses are generated by connecting an ultrasound transducer to a pulser circuit, and received by connecting an ultrasound transducer to a receiver circuit. The pulser circuit generates a very high voltage pulse with negative amplitude, which drives the transducer. The receiver circuit is designed for much lower voltages, and must be able to receive signals on

the scale of millivolts (mV). In the case of this project, the pulser circuit output and receiver circuit input will be connected to the same ultrasound transducer through a coaxial cable. This introduces another layer of complexity, as the receiver circuitry must be isolated from that of the pulser. The goal of this project is to design the pulser/receiver, which will then be connected to an ultrasound transducer through a coaxial cable. A rough sketch of the intended operation of the final device is shown below in Figure 2.

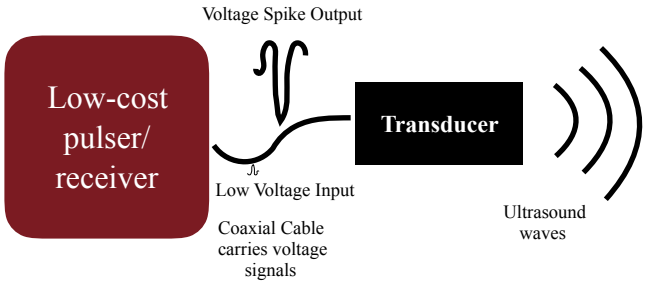


Figure 2: High-Level Sketch of Key Device Stages

The project will be designed in stages. The focus of the Fall Term was the pulser circuitry, with additional research being done into overall functionality and components. Preliminary research into the receiver circuitry was also completed. The receiver circuitry and the input adjustments will be the primary focus of the Winter Term. The overall device will also be planned and designed during the Winter Term. Eventually, each separate stage of the project will be combined into one single device that will plug into the wall outlet. The testing of this final device will be the focus of the remainder of the Winter Term, as well as the completion of the final report and presentation.

The remainder of this report includes the following. Section Two features background information on the topic and device. Section Three provides more detail about the design requirements, including a block diagram of individual stages. Section Four details design alternatives, and includes a component justification. Section Five discusses the design proposed

at the end of fall term. Section Six focuses on the actual final design implemented. Section Seven is a discussion of some preliminary results from the prototype design, the results from the final design, and a comparison of the two. Section Eight is a schedule of the design process followed over the course of the winter term. Section Nine provides a brief analysis of the costs associated with the device. Section Ten provides the user with an instruction manual for device operation and rudimentary troubleshooting. Section Eleven is a discussion of the project as a whole, various lessons learned, and recommendations of future work. Section Twelve provides a list of all references used throughout this report. Section Thirteen is comprised of various appendices referenced throughout the report or detailing work performed through other mediums.

2. BACKGROUND

2.1. Previous Research and Study

Because this project is largely constrained by cost, and because the final device will be a somewhat less functional version of a widely available device, there has not been a great deal of work done to find low-cost alternatives to the existing industry unit. One major investigation conducted about this particular problem was done by Jeremy A. Brown and Geoffrey R. Lockwood, but their study focused only upon the pulser circuitry and assumed that components such as the high voltage power supply and ultrasound transducer had already been purchased, and so did not factor these component costs into their budget [2]. Therefore, while their circuit appears to be fairly inexpensive, this project will also have to include the price of components necessary to the overall device that were not included in their paper. The need for both pulses out and reflections in to be transmitted along the same co-axial cable introduces the need for protection circuitry, as discussed by Jens Kristian Poulsen [3]. This paper examines various techniques that can be used to isolate the high voltage output pulse from the low voltage received, justifying the design and use of each individual technique.

Beyond the cost element, the paper by Brown and Lockwood discusses several other aspects and constraints of designing an ultrasound pulser. The amplitude of the pulse depth is dependent upon the voltage supply used to drive the power MOSFET. However, that pulse depth is also dependent upon the speed of the high-power MOSFET, to a degree as is the pulse width. They observed excess ringing immediately following the high-voltage pulse, but found it to be fairly negligible in comparison to the magnitude of the high-voltage pulse.. They also offered solutions to isolate the ringing if it was absolutely necessary to isolate the pulse from all excess

ringing. In their testing, they did not attempt to drive a load higher than 100 ohms (Ω), though they did find that it was possible to drive capacitive loads. The final prototype of their design could be used for ultrasound imaging purposes ranging from 1 to 60 megahertz (MHz) [2]. Their design is below in Figure 3.

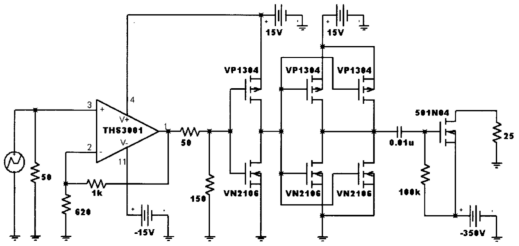


Figure 3: Brown and Lockwood's Pulser Circuit Schematic

Their design is quite simple, and was easy to simulate and prototype, though there were several further constraints not discussed in the paper itself. An external 0-5 V scale pulse is supposed to be amplified with an op-amp, the output of which is connected to the first of two inverting push-pull stages. The second stage consists of two N-channel and P-channel MOSFET push-pull stages in parallel with each other, which effectively doubles the current delivered to the high power MOSFET. Lastly, the high power MOSFET is what will output the high voltage pulse, with the drain connected directly to the load. These constraints include the dependence of the output pulse width on the input pulse width and the difficulty in outputting the appropriate amplitude from the op-amp sub-phase to turn the P-channel MOSFET fully on. As both of these characteristics are necessary in order for the device to function properly, these are major constraints to Brown and Lockwood's design that this project will attempt to remedy [2].

Since the pulser signal must be isolated from the receiver signal, it is also important to study and gain an understanding of protection circuitry. Poulsen discusses the use of diodes in order to ensure that the pulse signal is isolated from the receive signal. A diode expander is

connected to the pulser circuitry, allowing the high voltage pulse out, but preventing the receive pulse from returning into the pulser. Similarly, a diode limiter is connected before the pre-amplification stage of the receiver circuitry in order to allow the low voltage received pulse to reach the amplifier while preventing the high pulser voltage from reaching or destroying the receiver circuitry. This can be implemented with a capacitor, a 50 Ω resistor for impedance matching, or a transformer. Poulsen argues that the transformer is the best option, since it isolates the protection circuitry components from the initial high voltage pulse and provides better electrical matching between the transducer and the receiver circuitry [3]. The chosen protection circuitry is shown below in Figure 4.

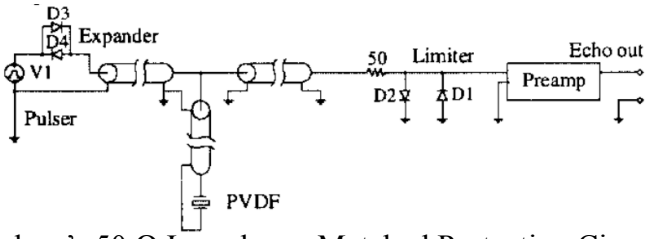


Figure 4: Poulsen's 50 Ω Impedance-Matched Protection Circuit Schematic

While the transformer protection circuit offers the most benefit, due to time constraints, the easier to implement 50 Ω impedance-matched option will be chosen.

One paper that discusses receiver circuitry for an ultrasound transducer is by L. Svilainis and V. Dumbrava. The pre-amplifier phase they design is meant to be used with ultrasound waves propagating through air, and closely examines the signal, the noise, and the signal to noise ratio (SNR). Through their work, they isolate some of the factors heavily involved in producing a great deal of noise. They also posit a few solutions to reducing noise, each dependent upon the parameter contributing the most to the noise. They note that their solution will not work for all ultrasound transducers, but they do provide a preliminary circuit that works with relatively low source impedance transducers [4]. The circuit they designed is shown in Figure 5, below.

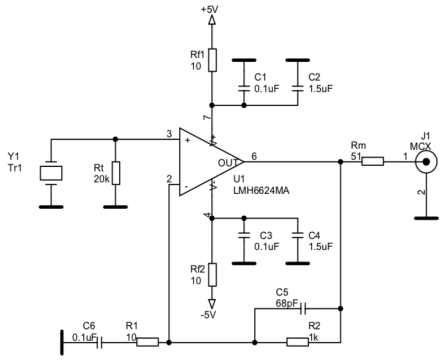


Figure 5: Preliminary Design of Pre-Amplification Stage of Receiver

Based upon the results they have achieved, new component values can be calculated and an appropriate pre-amplification circuit designed. The signal, noise, SNR, and other factors will have to be closely examined in order to begin these calculations.

2.2. Potential Project Impacts

The successful completion of this project would have a large positive impact on Professor Buma and his research. Even if he does not pursue replication of the project, having at least one additional ultrasound pulser/receiver with all necessary base functionality will allow him to image an additional subject without having to buy a new, more expensive device. The more successful the project is—the more high-level functions added to the overall design—would only continue to make this positive impact greater, as it would allow for more functionality or more precise imaging. Because the final design is expected to be fairly simple, it should also be easily replicable, meaning that should Professor Buma decide that one additional ultrasound device is not suitable for his needs, he should be able to quickly and easily construct another device, potentially even being able to alter some of the optional features to provide more or less functionality as appropriate.

While Professor Buma is the target of the project's positive impact, the low-cost design could also aid others who are interested in inexpensive ultrasound imaging solutions. There are surely other professors here at Union who rely heavily upon ultrasound imaging when conducting their research who could be positively impacted by the existence of a low-cost alternative to more expensive devices. The final design will be well labeled and easy to pick up and use, even for those unfamiliar with circuitry. This is a large factor in the final design, as the final device should function similarly to the industry device in that it should be self-contained, with the only connections extending to power, the input/output cable, and an external trigger. If it is externally similar to the industry device, it will be easy for anyone familiar with the proper operation of that device to use the final device created through this project.

Regardless of the state of the final project, it can also aid future students in learning more about how ultrasound pulsers and receivers work. Students can study the final design itself if they are interested in learning more about practical applications of circuit design, but can also easily repeat the design and conduct their own tests and improvements upon it. Depending upon the level of additional features, this project could be expanded or improved upon by future capstone students. Because of the many individual functionality improvements, it is very easy to add additional features to the final design, as well as remove other features.

There should be no ethical issues associated with the deign or use of this project. Because ultrasound imaging is often conducted on living beings, it should be safe to use and pose no threat of electrical shock to either the user or the subject. Legally, it should comply with the same codes and standards as the industry device. This includes the IEEE standards of ethics and the industry requirements for high-voltage devices. So long as care is taken to isolate the high

voltage supply and other dangerous concerns, the final device should be able to comply with these standards easily. As the entire device is enclosed in a box with no unsafe outlets, this should not pose a problem.

3. DESIGN REQUIREMENTS

In order for this device to be considered successful and functional, it must meet a series of design requirements, which are outlined below. Most of these requirements were defined based upon Professor Buma's requests, as he is the target customer of the final device. The requirements are broken up into three categories: requirements that apply only to the pulser, requirements that apply only to the receiver, and requirements that apply to the overall system.

3.1. Design Requirements for Pulser Stage

The pulser stage is the primary focus of the project, as its requirements will have the greatest impact on the overall device. There are two levels of requirements, those that are absolutely necessary for the device to work, and those that are desired for higher levels of functionality, but not absolutely necessary to the device's basic functionality. The high-level requirements are still strongly desired by the customer, but not meeting them will not mean the project as a whole has failed.

3.1.1. Base Requirements for Pulser Stage

The pulser stage includes a set of requirements that are necessary in order to ensure basic functionality of the overall system. Most importantly, the pulser must be able to create a negative voltage spike of at least 150 V. The width of this pulse should be less than 100 nanoseconds (ns). The repetition rate of the output pulse shall be approximately 1 kHz. An external trigger is required so the device is informed about when to output a pulse. When the device receives this trigger, it should be able to output the negative voltage spike. The external trigger will operate on a 0-5 volt logic scale, so the pulser should be designed to receive a 5 volt input. The output load of the pulser, the ultrasound transducer, can be modeled with an

impedance of approximately 50 Ω. The output of the pulser will also be connected to the receiver circuitry, also designed for an output impedance of 50 Ω. When the pulser is on, these two loads will appear to be in parallel, making 25 Ω an appropriate choice to model the pulser behavior of the final device during pulser-only testing phases.

3.1.2. High-Level Requirements for Pulser Stage

After basic functionality is confirmed, additional functions will be added and tested to the overall circuitry. These additional functions are primarily input adjustments, changes that can be made before any signal has been sent to the device, that will affect the final shape or behavior of the output pulse. The repetition rate shall be adjustable, ideally up to 20 kHz, but 5-10 kHz would be considered an acceptable value. An option for an internal trigger that would keep time and trigger the device without additional input is also highly desired.

3.2. Design Requirements for Receiver Stage

The biggest concern related to the receiver circuitry is the shared connection to the coaxial cable connected to the ultrasound transducer. The transducer requires a very high voltage pulse to transmit ultrasound waves, but will return a comparatively very low voltage signal to the device. The receiver must be protected from the pulser's output spike but still be able to detect the very low voltage reflected back to the device. The signal returned by the transducer will be on the scale a few mV, and must be amplified so that it can be viewed on an oscilloscope or other signal visualizer.

3.3. Design Requirements for Overall Device

Like the pulser, the final device has some basic requirements and some requirements that are not absolutely necessary to the device's overall function but desired by the customer. Unlike

the case of the pulser, however; not meeting these requirements can severely limit the final functionality of the device, so while they are higher level requirements, they should also be met.

3.3.1. Base Requirements for Overall Device

Though it is not a technical requirement, one very important overall requirement of the device's design is cost. As the device is supposed to be a low-cost alternative, it should not be cost-prohibitive to construct. The device is also limited by the Student Research Grant program; the project has been approved for a $399 budget. The original SRG proposal and award letter are attached in Appendices A and B.

The high voltage output means that electrical safety must be paid careful attention to, so the current flowing through and the power dissipated by the device do not cause harm to the user. The current flow and power dissipation must be closely monitored in order to ensure the safety of both the user and the subject. The device should be able to meet all the standards of electrical safety that the industry device can, including IEEE ethics and industry safety requirements..

The final device shall behave like Professor Buma's more expensive device, meaning that it will run off the AC wall line and have the appropriate BNC input/output connections. It should be of similar dimensions and weight, though there are no specific size and weight constraints on the device.

3.3.2. High-Level Requirements for Overall Device

The device's circuitry shall be implemented through the use of a Printed Circuit Board (PCB). The use of a PCB will allow for ease of repeatability, should Professor Buma desire to replicate the device. The use of a PCB would also make for faster connections, and therefore a more stable output pulse. This is a future concern, but it will improve the functionality greatly.

The device should ultimately be mounted on a metal housing or similar casing, with appropriate input and output connections. The size of this final device should not be much larger than the original device, which is 7 inches wide by 3.5 inches tall by 9.1 inches long, but the physical size of the device is not an immediate concern [1].

4. DESIGN ALTERNATIVES

Several different components were chosen for this project, and some are still in the process of being decided upon. The pulser components are essentially finalized, as are some of the overarching components. The receiver components have not yet been finalized, but the general parts necessary have been determined. This section is broken up similarly to the previous section, with each subsection detailing the parts most relevant to the design.

4.1. Component Alternatives and Justifications

Many alternatives were considered, and in some cases tested, before they were ultimately decided against. The most specific design is the pulser circuit, as the general design has been finalized. The specific components must be replaced and tested for optimization. The receiver circuit has been designed with a general idea of necessary parts, and several overall components are currently being chosen. This section is broken up by these three categories in order to distinguish which parts are most relevant to which phase of the design.

4.1.1. Pulser Design Component Alternatives and Justifications

The pulser circuit was originally constructed based upon Brown and Lockwood's paper, using the parts available within the ECBE department. This meant that the op-amp was lower powered and slower, the power MOSFET could not handle the same current, and the other MOSFETs had different ratings. Instead of the THS3001 op-amp [5] suggested by the paper [2], the breadboarded prototype was constructed using an LF356N [6]. Instead of the 501N04A power MOSFET [7], the prototype was constructed using an IRF510 [8]. While the BS170 N-channel MOSFET [9] was not the same as the one suggested by the paper, the VN2106 [10], they had similar characteristics, and therefore using alternate components should not have a large

effect on the overall design. The P-channel MOSFET available for use, the VP2106 [11], was the same as the one suggested by the paper, and functioned as expected when paired with the BS170 N-channel MOSFET.

Minimal testing was done on this prototype, but during these tests, it was observed that the output pulse width was dependent upon the input pulse width. This is because using an op-amp only amplified the input pulse's amplitude, but did nothing to change the width. Since Professor Buma desired the final output width to be fixed, this design could not be used. Therefore, the SN74HC00N high-speed 4-gate NAND chip [12] was used instead, as the pulse width could be set by taking advantage of the inherent propagation delay of digital logic. This high-speed chip was chosen over its lower-speed counterpart in order to limit the propagation delay caused by the logic chip. This produced the desired final pulse width behavior, with the final pulse width being dependent upon the value of the delay resistor. While the final pulse width is not significantly lower than 100 ns, it is no longer reliant upon the input pulse width.

Because both the VN2106 and the BS170 N-channel MOSFETs have similar characteristics [9] [10], mainly a maximum drain-source voltage of +60 V and an average turn-on time of 7ns, and the VP2106 P-channel MOSFET can be replaced with other MOSFETs with similar characteristics, it was determined that the final choice of MOSFET for the push-pull switch was not largely important, so long as the MOSFETs chosen could achieve this desired behavior. The deciding factor in this case will be cost, and since the ECBE department has multiple BS170s and often uses VP2106s, these will be the components used for the push-pull switches. The push-pull stages are not incredibly demanding on the overall system, nor do they

require a high voltage, current, or power tolerance, so the choice to use the BS170 and VP2106 MOSFETs will not have a great effect on the overall circuit performance [9] [11].

The final power MOSFET is incredibly important, as it allows for the high voltage pulse to be output. If it cannot react quickly enough or withstand the high power dissipated across it, the final output pulse will not behave as expected and the overall device could even malfunction or break. The 501N04A chosen by Brown and Lockwood is rated at 500 V, 4.5 A, and has turn-on and turn-off times of 4 ns each [7]. Their paper discussed a design meant to handle -350 V and greater, but since the maximum voltage that will be dissipated across this power MOSFET is only around -150 V, the power MOSFET used does not have to be withstand such a high voltage rating. The most important factor in the choice of the power MOSFET is the turn-on and turn-off times, as these are what will affect the output pulse the most. The 201N09A power MOSFET has a turn-on time of 4 ns and a turn-off time of 4 ns, and is rated for 200 V and 9 A, making it more than sufficient for this application [13].

4.1.2. Receiver Design Components and Justifications

The receiver design consists of the protection circuitry and pre-amplification stage. The protection circuitry will consist of 2 diodes, each of which must be able to withstand the brief, approximately 3 ampere (A) current caused by the high voltage pulse. This current was calculated by using the magnitude of the high voltage pulse, 150 V, and the characteristic impedance of the pulser circuitry, 50 Ω. This current will be a major factor in the determination of several parts beyond just the protection diode. The impedance-matching resistors must also be able to withstand the power dissipation caused by the 3 A pulse. The diodes are the most important, however; since if the protection circuitry fails, the receiver circuitry can be damaged

by the very high voltage and associated power dissipation. This sub-phase of the design will likely see the highest power dissipation, and the final design must account for those constraints.

The receiver pre-amplification circuitry makes use of an op-amp to amplify the signal received from the ultrasound transducer and reduce the noise received. The way that this op-amp is applied will drastically change the overall performance of the receiver circuitry. Svilainis and Dumbrava warn against excessive amounts of DC bias, suggesting that the amplifier feedback loop be broken in order to eliminate the problem of DC bias voltage [4]. This pre-amplification phase does not provide a great deal of amplification on its own, but it successfully removes a great deal of the signal noise from the received signal. This less noisy signal can then be passed to a proper amplification stage, also consisting of an op amp, in order to examine the received signal.

4.1.3. Overall Design Component Alternatives and Justifications

The biggest task of the Fall Term was determining an appropriate high voltage power supply. This high voltage power supply also had the majority of the SRG budget devoted to it. The original SRG proposal included an unregulated DC power supply unit by Acopian [14]. This model was designed to plug into the wall and deliver a semi-steady single output voltage. This was ultimately decided against because the unregulated nature of the supply meant that there would not be a constant voltage level delivered to the source of MOSFET, but a varied value averaging the advertised value of the power supply, which would not be conducive to a consistent pulse depth or width. After this power supply was decided against, research was conducted into on-board power supplies. One was found that was fairly small in size, but it had no means to quickly deliver a large amount of current in a short amount of time [15]. Because of

this limitation of the otherwise appropriate supply, it was ultimately decided that the power supply need not be an on-board module. Studying the Acopian models again, a regulated high voltage DC power supply was found. This model can output 150 V and 100 mA [16]. While the use of this model is not as ideal as having an on-board connection, it will be much easier to incorporate this into the overall design, especially when time constraints are taken into account.

The overall device will be powered by a +15 V wall line adapter. This voltage will be used to power the majority of the device, save for the high voltage pulse output. This value will have to be adjusted for the NAND gate chip, as it takes +5 V to power the chip [12]. The push-pull switches and the receiver circuitry will all be powered directly by the +15 V source.

5. PRELIMINARY PROPOSED DESIGN

The overall device has four distinct phases, each with several sub-phases. These phases are detailed in the block diagram shown in Figure 6, below. The input adjustments mostly cover the high-level requirements discussed in Section 3. The focus of this term was obtaining SRG funding, building and modifying Brown and Lockwood's pulser circuit, and testing the new pulser design. The receiver circuitry had not been fully designed at the end of the fall term, and only some preliminary research into the overall design had been conducted. Each phase of the design has its own section, which will discuss various aspects of the current design and potential future steps. The pulser design phase is also broken up into subsections, each discussing different design phases. This section was written at the end of the fall term of 2018, and was focused upon summarizing the work done and preparing for the work to be done in the winter term of 2019.

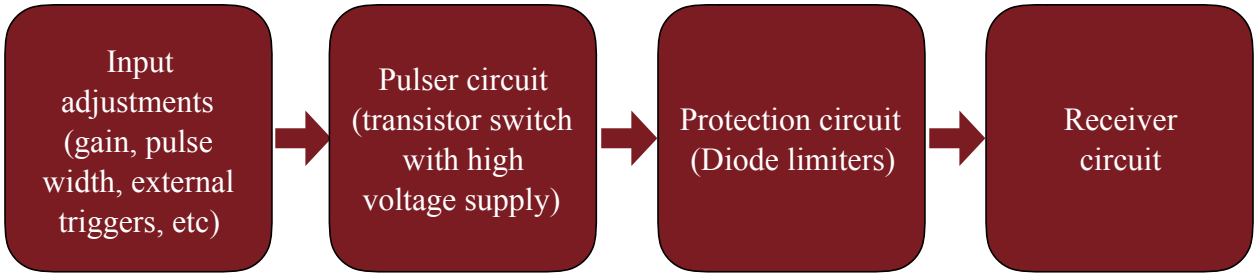


Figure 6: Preliminary Block Diagram of Overall Device (Following Signal Path)

5.1. Pulser Design

During the fall term, the pulser design went through three distinct design and pseudo testing phases. Firstly, the circuit proposed by Brown and Lockwood was constructed and cursorily tested. Some modifications were made to that circuit, which resulted in the current circuit design. A breadboarded version of this circuit was constructed and tested more fully than the preliminary design. The preliminary results of this phase were presented during Week 9 of

the fall term. This poster presentation is included in Appendix C. Since then, that same circuit has been soldered on a perfboard in order to create a very basic prototype of the pulser circuit.

5.1.1. Brown and Lockwood's Design

Brown and Lockwood's design consisted of three phases, detailed by the block diagram below, in Figure 7. The circuit itself is discussed in Section 2, and shown in Figure 3.

Figure 7: Block Diagram of Brown and Lockwood's Circuit

The circuit was constructed using the available parts in the ECBE department, which meant that the final prototyped circuit would not be as functional as the one described in the paper. However, this preliminary construction was enough to begin testing the pulser circuit and considering alternative designs. A final output pulse was never achieved with this design, and no oscilloscope traces were saved before the breadboarded circuit was altered to implement digital logic. A key flaw in this design that led to the consideration of other pulse generator options was the dependence of the output pulse width on the input pulse width.

5.1.2. Breadboarded Digital Logic Circuit

The digital logic pulser circuit can be broken down into four distinct phases. A block diagram of these phases is shown below in Figure 8. Circuit diagrams are included and discussed in Section 6.

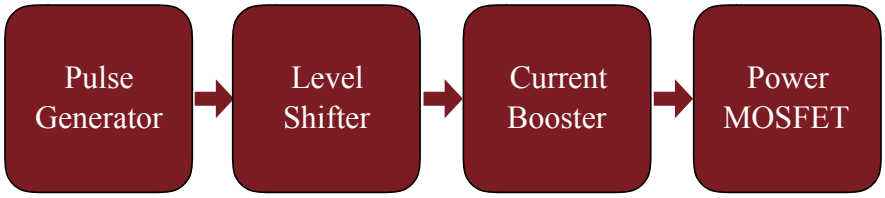


Figure 8: Block Diagram of Digital Logic Pulser Circuit

The additional phase, as compared to the previous design, is the level shifter, which is necessary to ensure that the output of the NAND logic phase is a high enough input voltage for the push-pull MOSFET phase. Because the level shifter inverts the signal again, an additional inverting push-pull stage is also necessary. Figure 9, below, is an image of this breadboarded circuit.

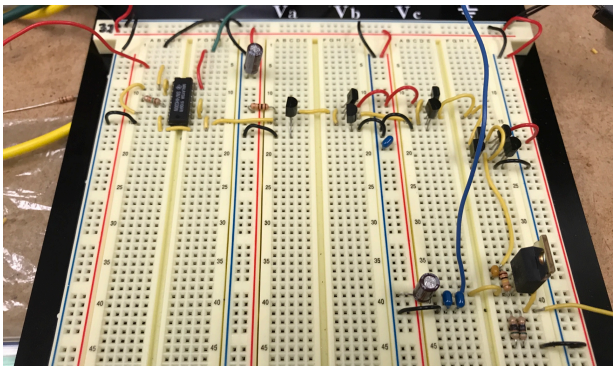


Figure 9: Breadboarded Digital Logic Circuit

Professor Buma suggested the use of digital logic gates. This meant that the amount of time the output of any given logic gate was high could be controlled by the inherent propagation delay of digital logic. A NAND gate was chosen because this implementation required inverting the signal at various stages. Because of how NAND logic works, tying the inputs of a NAND gate together functionally acts as an inverter.

The input pulse signal is fed into three pins of the SN74HC00N NAND chip—pins 1, 2, and 5. Pins 1 and 2 are connected to the same NAND gate, considered as Gate 1 by the datasheet [12]. and therefore simply invert the input signal. This inversion stage is used to introduce more delay. The output of Gate 1, pin 3 is tied to the input of Gate 2, pin 4. Theoretically, the delay caused by this inversion should produce a noticeable difference in “high” level time and cause the pulse width at the output of Gate 2, pin 6, to be much shorter than the original input pulse. A demonstration of the desired response is shown on the next page in Figures 10 and 11.

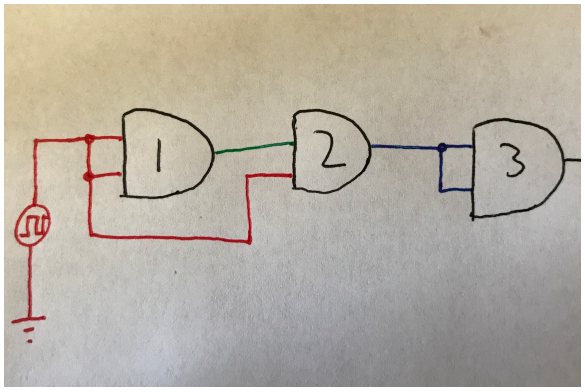


Figure 10: NAND Gate Schematic with Inherent Propagation Delay

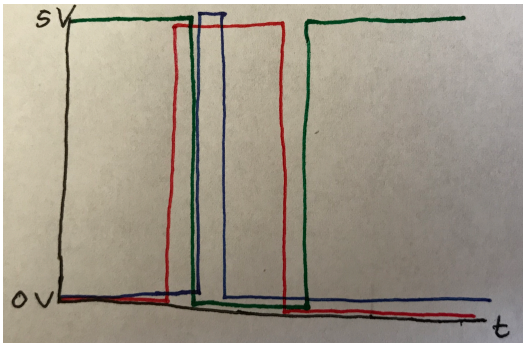


Figure 11: Timing Diagram of Inherent Propagation Delay

However, the propagation delay of this inversion is not long enough to produce a noticeable overlap in signal "high" levels. During breadboard testing, a resistor was introduced between pins 3 and 4 in order to "slow down" the signal response. A demonstration of this "slow down" method is shown below in Figures 12 and 13.

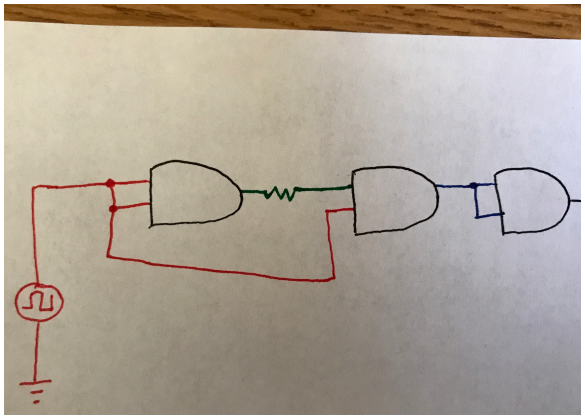


Figure 12: NAND Gate Schematic with Delay Resistor

Figure 13: Timing Diagram of Delay Resistor

This should cause the input signal to pin 4 to dissipate more slowly than a direct connection, meaning that the input pins to Gate 2, pins 4 and 5, will see a more noticeable overlap in "high" times, causing the final output of Gate 2, located at pin 6, to be shorter than the input pulse, but still detectable and able to be carried forward. The "slowed down" signal can be seen in the green trace and the blue trace is the resultant shortened signal output. This signal should be a positive voltage pulse of around 5 V and 60 ns.

Pin 6 is then connected to pins 10 and 11, the input pins to Gate 4. This stage is necessary in order to make the final output of the NAND gate pulse generator phase a positive voltage pulse. The final output of the NAND gate pulse generator should be a positive voltage pulse of around 5 V and 60 ns.

This output voltage is then delivered to the gate of the BS170 N-channel MOSFET. Using a 100 Ω resistor between +15 V V_{CC} and the source allowed for the 5 V at the gate to turn on the MOSFET, causing the source voltage to reach the 15 volt output level required for later circuit phases. This resistor is necessary because it allows the signal to be carried further through the circuit. Because this level shifter uses a MOSFET, it also inverts the signal.

The current booster phase consists of two inverting push-pull MOSFET switches connected in series. Each stage consists of a BS170 N-channel MOSFET and a VP2016 P-channel MOSFET. The gates of the N-channel and P-channel MOSFETs are tied to each other, as are the drains. The input signal is fed into the gates, and the output signal is measured from the drains. The source of the N-channel MOSFET is connected to ground, while the source of the P-channel MOSFET is connected to the positive supply, +15 V V_{CC}, as the N-channel MOSFET was in the previous level shifting phase. These first two stages are used to increase signal stability and marginally decrease signal width. The first push-pull stage produces a positive output, and the second produces a negative output. This negative output is then connected to a third push-pull stage. This third stage consists of two inverting push-pull MOSFET switches in parallel with each other, effectively doubling the current. All connections are the same as with the push-pull switches previously discussed, with the only difference being the direct parallel connection to the second push-pull switch. This final stage is necessary in order to ensure that the

gate of the power MOSFET receives enough current to turn on or off. The final output of this stage is a positive pulse of approximately 15 V and 60 ns. This 15 V pulse is enough to turn on the high power MOSFET because it is above the turn-on threshold of 4.5 V and provides enough current to the gate of the high power MOSFET.

The final IRF510 power MOSFET phase produces the desired negative voltage pulse. Between this phase and the current boosting phase is a capacitor, which isolates the voltage pulse from the output of the previous stage and centers it around $-V_{CC}$, which has typically been set at -30 V for the recording of oscilloscope traces. $-V_{CC}$ is the gate voltage of the power MOSFET at all times except when the input signal has been carried through the pulser circuit and has passed through the capacitor. The capacitor is connected to the gate of the power MOSFET. The source of the power MOSFET is connected to the negative supply, $-V_{CC}$. It is also connected to the drain through a 100 kΩ resistor. The drain is connected through the output resistor, modeling an ultrasound transducer assumed to have an impedance of 50 Ω, to ground. It is the output of the drain that is considered the final output and has been measured as such. The final output of this phase, and the pulser as a whole, should be a negative voltage spike with a magnitude of $-V_{CC}$ and less than 100 ns, which has been mentioned as the maximum pulse width that will be able to drive an ultrasound transducer in Section 3.1.1. The final pulse depends upon the value chosen for $-V_{CC}$. In this case, the IRF510 is not rated for voltages over 100 V, and so $-V_{CC}$ should not surpass that value during testing, in order to protect the power MOSFET.

5.1.3. Soldered Digital Logic Circuit

Based upon the performance of the breadboarded circuit, it became clear that further optimization of the signal was necessary. It was posited that some of this optimization would

result from constructing a soldered prototype. The soldered prototype circuit was laid out identically to the breadboarded circuit and included single pin sockets to allow for ease of replacing the delay and load resistors. The ability to change the delay resistor was crucial, as the propagation time of the NAND chip was found to be greatly decreased upon measurement of the soldered prototype. Additionally, it was found that varying the value of this resistor would vary the final output pulse width, with a higher resistance corresponding to a longer pulse duration. An image of the current soldered prototype is shown below in Figure 14.

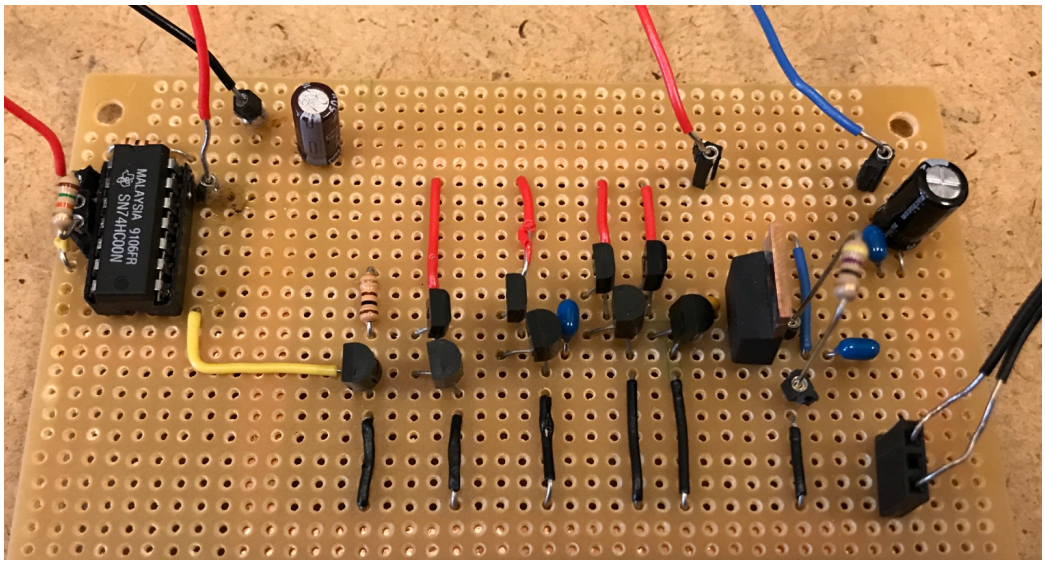


Figure 14: Soldered Digital Logic Circuit

The current soldered prototype was constructed using parts available within the ECBE department, so some will be replaced by the time the final design is implemented. The IRF510 power MOSFET will be replaced with the 201N09A power MOSFET in the final device. The other components will likely not be replaced, as they have been chosen for use in the final device. One major difference between the current model and the final model is the current prototype's reliance upon an external power supply. Since the final device will be self-contained, the high voltage supply will either be on board the board itself or contained within the device

housing. Since a goal of the project is to implement it using a PCB, the final device will not be constructed on a perfboard, and will likely look quite different. However, the general layout of the circuit and the various components, in a general sense, will be used in the final pulser design.

5.2. Receiver Design

During the fall term, designing the receiver circuitry was not a large focus, so there is not a great deal of information pertaining to this design. General research into its design and functionality has been conducted, however; and it has been determined that it will consist of the following stages: protection circuitry, a pre-amplification phase, and a final amplification phase, illustrated in the block diagram shown in Figure 15, below.

Figure 15: Block Diagram of Receiver Circuit

Specific parts have not yet been chosen, but aside from the protection circuitry, this design should not be immensely complicated or demanding. Svilainis and Dumbrava's circuit will be used in the preliminary design [4]. This design was not simulated during the fall term, and would have been simulated in the first weeks of the winter term, but the receiver portion of the project was ultimately cut from the scope of the project due to time constraints. The most important factor of this design is ensuring that the protection circuitry is able to withstand the high power dissipation and isolate the high voltage signals from the more delicate receiver circuitry.

5.3. Overall Design

The overall design itself has not yet been considered, but research into various components that will affect the overall device has been conducted. Because of the choice of high-voltage power supply, the final enclosure will be quite large, as it must encompass both the wall-line module and the device. This will result in two separate power cables, one to power the high-voltage supply, and one to power the device itself. Additionally, the final device must have a BNC connector for input/output and a BNC connector for external triggering. The goal of the project is still to make use of a PCB for the pulser/receiver circuitry and to enclose the entire device in a metal housing, making it appear similar to the industry standard device.

6. FINAL DESIGN AND IMPLEMENTATION

The final design consisted of five primary stages, outlined in the subsections to follow. Several changes were made from the preliminary design proposed in Section 5, which are detailed in a subsection preceding the final design choices made. Next, this section features a subsection on how the appropriate voltage and current levels were delivered to each component. Finally, this section discusses the importance of device housing and the factors that led to the final choice of container.

6.1. Changes from Preliminary Design

The biggest change in the device design from that proposed in the previous section is the removal of the receiver stage. Due to time constraints, the receiver portion of this project was removed, and the focus shifted to only designing and implementing the pulser. The final project essentially only focused on designing the pulser stage and making it function as closely to the base requirements as possible, in order to compensate for the inability to meet other goals. Additionally, the project was never implemented on a PCB, only a perfboard, also due to time constraints. Aside from that, the biggest change from the proposed and prototyped design was the addition of an internal oscillator and the use of the proposed components rather than less powerful or high functioning stand-ins.

6.2. Pulser Design

The final pulser design is quite similar to the proposed design, but several changes were made in order to meet the initial goals of the project. This mostly consisted of designing the internal trigger method, adjusting various component values, and some small changes to the final stage of the pulser circuit. Several other initial design expectations were not met or designed for

due to the time constraints of the project. More information on these changes is detailed within the subsections to follow.

6.2.1. Internal Oscillator

The internal oscillator was necessary in order for the device to self-trigger. This means that the device had only to be turned on to begin outputting the pulse to drive an ultrasound transducer. Three different methods were discussed: (1) starting with a high clock and dividing down, (2) a 555 timer, and (3) a simple NAND gate oscillator. Method (1) was decided against because I did not have a decade counter, nor time to purchase it. Method (2) was pursued and two different circuits prototyped, while method (3) had only one prototype. Ultimately, Method (3) was chosen because it provided the most stable behavior and its behavior most closely matched the predicted behavior.

For Method (2), an astable pulse generator with a non-50% duty cycle and an astable pulse generator with a 50% duty cycle were both tested [17]. Neither circuit behaved as formulas predicted, so alternate routes were pursued. In both diagrams, C2 is used only to set the threshold, and was prototyped using the fixed value of .01 uF. The circuit schematics are shown below in Figures 16 and 17.

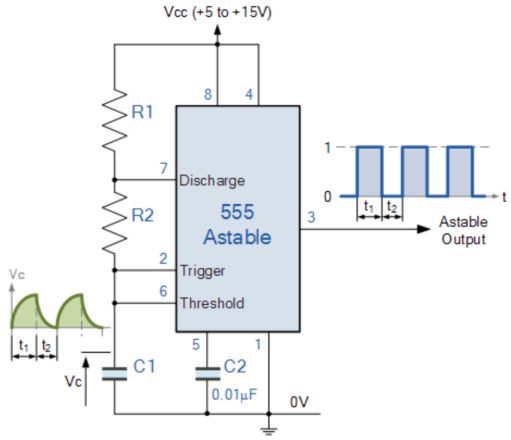


Figure 16: Astable 555 Timer Schematic (Non-50% Duty Cycle)

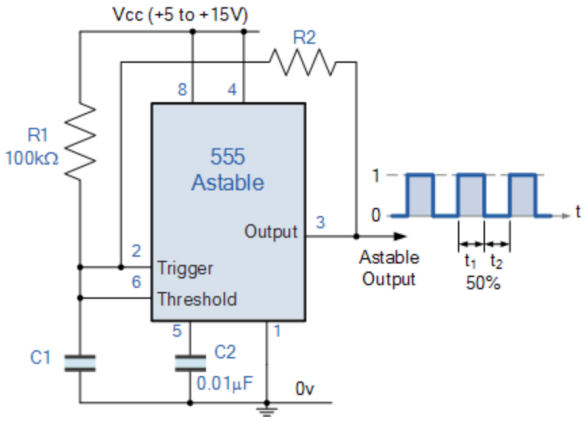


Figure 17: Astable 555 Timer Schematic (50% Duty Cycle)

The non-50% duty cycle 555 timer uses every pin of the 555 timer integrated circuit, while the 50% duty cycle timer does not use pin 7, the discharge pin, as C1 now charges and discharges through the same resistor, R2. The equation used to determine the component values for the non-50% duty cycle 555 timer is shown below in Equation 1. For a 1kHz repetition rate, C was set to be 100 nF, R1 was mathematically determined to be 7.5 kΩ, and R2 3.3 kΩ.

$$f=\frac{1.44}{(R1+2R2)*C} \tag{1}$$

The equation used to determine the component values for the 50% duty cycle 555 timer is shown below in Equation 2. The value of R1 ensures the capacitor charges fully, and must be high enough so that it does not interfere with charging of the resistor, and was tested at 100 kΩ. C was again set to be 100 nF, with R2 being mathematically determined to be 7.5 kΩ.

$$f=\frac{1}{0.693*2R2*C} \tag{2}$$

Method (3), the simple NAND gate oscillator was quite easy to prototype and behaved as predicted, and so therefore was selected as the most logical method of internal oscillation [18]. A schematic of this oscillator is shown below in Figure 18.

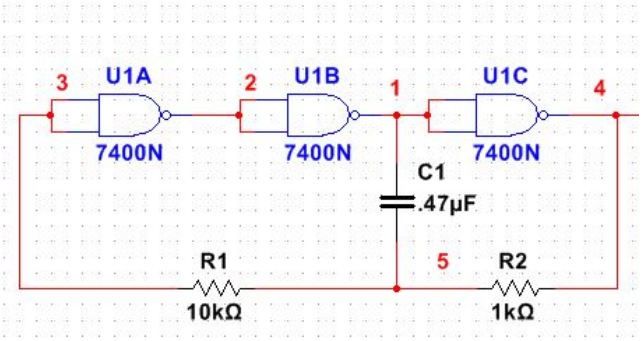


Figure 18: Schematic of Simple NAND Gate Oscillator

The equation used to determine the component values for the NAND gate oscillator is shown below in Equation 3. R1 should be set to be approximately 10 times R2.

$$f=\frac{1}{2.2*R2*C} \tag{3}$$

Solving this equation for a 1 kHz repetition rate, C was determined to be .47 uF and R2 to be 1 kΩ. Based upon this value of R1, R2 was then set to be 10 kΩ. This method proved to provide the output most closely matching the expected performance when prototyped, and consequently was the method chosen to provide the internal oscillation.

6.2.2. Low Voltage Pulse Generator

The low voltage pulse generator used in the final design was the same as that proposed in the initial design, but the value of the delay resistor was changed to the lowest value that could still produce a high enough voltage pulse to trigger the high power MOSFET after the signal traveled through the rest of the circuit. A schematic of the low voltage pulse generator is shown below in Figure 19.

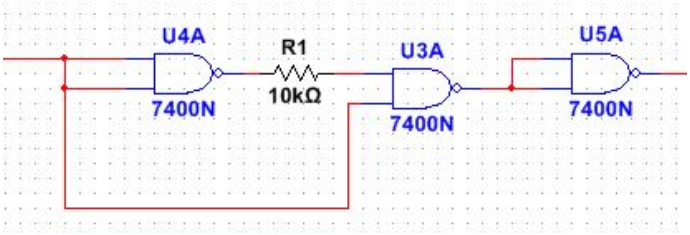


Figure 19: Schematic of Low Voltage Pulse Generator

6.2.3. Level Shifter

No changes to the level shifter stage were made from the preliminary design, as it was successfully working to shift the magnitude of the pulse from 5 V to 15 V. A schematic of both the level shifter is shown below in Figure 20, circled in red.

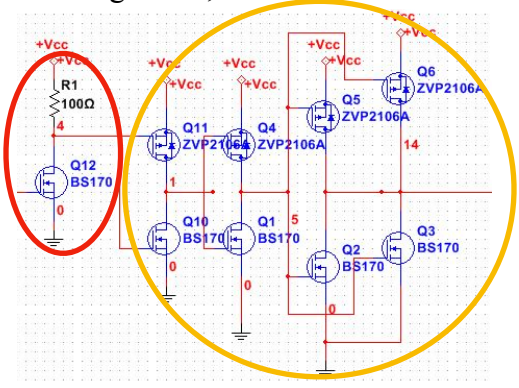


Figure 20: Schematic of Level Shifter (Circled in Red) and Current Booster (Circled in Orange)

6.2.4. Current Booster

The current booster stage was also not changed from the preliminary design, as the inverting push-pull stages were still capable of producing the desired output and the final current boosting parallel push-pull pair was able to output enough current, 180 mA, to turn on the gate of the power MOSFET. The current booster is shown on the previous page in Figure 20, circled in orange.

6.2.5. High Voltage Pulse Generator

The biggest change from the preliminary design was made in the high voltage pulse generator stage. The original design would have required a great deal of current (3 A) to be delivered by the high voltage power source. This 3 A current would be needed during the brief time the power MOSFET is on, and would be conducted across the 50 Ω load (used to model the 50 Ω impedance of a typical BNC cable). This would not pose a problem if the device was supposed to be plugged into another device, but as the goal was for the final device to be self-contained, the high voltage power supplies had to be housed onboard the device. Most relatively low-cost high voltage power supplies cannot output more than .5 A; the Acopian B150GT10 ordered can produce only .1 A. Also produced by Acopian, the A150HT300 can output 3 A, but this performance is drastically dependent on temperature (a 15° C increase drops this output to 2.5 A), and costs $720, almost 3 times more than the B150GT10 model (at $245).

Therefore, the need for an alternative design becomes clear. The B150GT10 can still be used, but it cannot be used to deliver current to the power MOSFET. The B150GT10 also is a positive output supply and the ultrasound transducer requires a negative pulse. Luckily, both these problems can be solved with the same method: the implementation of a high voltage

capacitor with a very high dV/dt. The 100 nF capacitor chosen was the CDE 715P10452LD3, with a dV/dt of 1100 [19].This means that the capacitor will be delivering the high current and through the way it is implemented, can also produce the negative voltage value necessary to drive the high voltage pulse out. A schematic of the circuit is shown below in Figure 21.

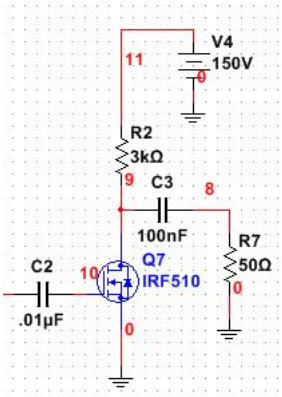


Figure 21: Schematic of High Voltage Pulse Generator

When the high power MOSFET is off, the capacitor is being charged. The 3 kΩ resistor limits both the charging speed and the current draw, but not to the point of compromising performance. The capacitor is able to fully recharge to 150 V within the 1 kHz repetition cycle, and the current draw from the high voltage power supply is limited to 50 mA, half of what it is rated for. During this charging phase, the drain voltage is 150, and the voltage across the 50 Ω is zero. When the power MOSFET turns on, current quickly rushes from the drain of the MOSFET to the source and the drain voltage becomes close to zero. The capacitor is quickly discharged, and the voltage across the load is -150 V. In this way, the desired output behavior is still achieved in a way that does not drastically increase the cost or complexity of the circuit.

The output of every pulser stage is shown on the next page in Figure 22, which includes every stage but the high voltage ones in order to make the individual pulses easier to see, and the high voltage pulses are shown on the next page in Figure 23, which are isolated for scale.

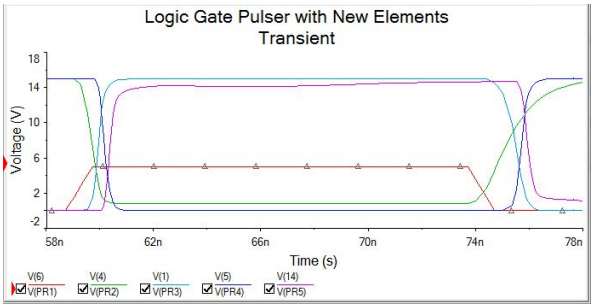


Figure 22: Comparison of Expected Circuit Outputs at Various Stages

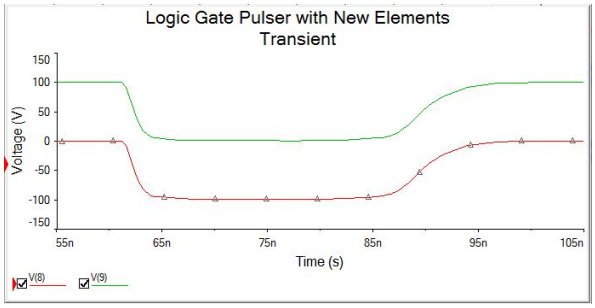


Figure 23: Comparison of Expected High Voltage Circuit Outputs

In Figure 22, the red trace is the expected low voltage pulse generator output, which is a +5 V pulse, the green trace the expected level shifter output, a -15 V pulse, the teal trace the expected output of the first inverting push-pull stage +15 V pulse, a, the blue trace the expected output of the second inverting push-pull stage, a -15 V pulse, and the purple trace the expected output of the current booster stage, a +15 V pulse. In Figure 23, the green trace is the expected voltage at the drain of the high power MOSFET, a -100 V trace centered around 100 V, and the red trace the expected voltage across the output load, here modeled as a 50 Ω resistor, a -100 V trace centered around 0 V. The simulation was run using an IRF510, whose maximum drain-source voltage is 100 V, so the pulse only reaches -100V, but is in fact achieving the full pulse depth it can produce. When the 201N09A is implemented in the final device, it is expected that it will be able to reach the full -150 V pulse depth, as its drain-source voltage is 200 V, more than sufficient for the expected performance.

6.3. Power Delivery Methods

Because the device was to be self-contained and connected to the wall, the AC line voltage had to be converted to the appropriate regulated DC voltage levels. Three different DC voltages were required, +150 V to drive the final output, +15 V to drive the intermediate MOSFETs, and +5 V to drive the digital logic chips. As discussed previously, the B150GT10

was used to obtain the +150 V. The Acopian device simply had to be connected to the AC live and neutral, as well as earth ground, and could produce a stable +150 V output.

The +15 V and +5 V outputs were not quite as simple to obtain as the +150 V output, but did not require a great deal of effort. Like the +150 V output, these voltages had to be adapted from the wall line. In order to step down the 120 VAC wall voltage, the Hammond BD2EE transformer was used, which took the 120 VRMS input and output 14 VRMS [20]. The output of the transformer was then connected to a voltage regulator with capacitor filtering, which gives a semi-stable +20 V output. This 20 V output was then connected to a LM317 voltage regulator, configured for a stable +15 V output. In order to achieve the +5 V output, the +15 V output was connected to a LM7805C voltage regulator, this time configured for a constant +5 V output.

Though it is not shown in the schematic, fuses were included just after the wall input live and neutral line connections to protect both the device components and anyone who my inadvertently come in contact with current-carrying wires from current overdraw. 5 x 20 mm slow-blow cartridge fuses at a value of 250 mA were chosen for their ease of implementation and interchangeability. One simply has to connect the fuse holder in series wherever the fuse is desired and this type of casing makes it very simple to change out fuses that have blown or that are an incorrect value. 250 mA is actually somewhat high, as the total estimated current draw of the device is just under 200 mA, but there was not time to obtain and test other fuses. Also not included in the schematic is a power switch, which provides the user a way to remain safe, as the device will not begin drawing power until the switch is turned on. The appropriate power circuitry outputs were connected to the pulser components in order to power them. A schematic of the power circuitry, excluding the +150 V DC, is shown on the next page in Figure 24.

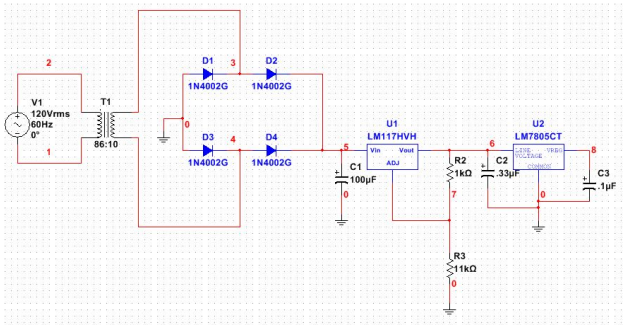


Figure 24: Schematic of Power Circuitry Used to Obtain +15 V DC and +5 V DC outputs

6.4. Device Housing

The overall device was constructed on three perfboards, two 3.125” L x 4.25” W and one 2” L x 2.5” W. These perfboards, as well as the Acopian B150GT10 and the Hammond BD2EE transformer were all housed in the Hammond 1426Q steel box. The box was 11.75” L x 11” W x 5.5” H, which was somewhat overlarge for the various components, but which also allowed for plenty of options in the final device layout. The way the device was constructed with power-related elements toward the back of the device, closer to the power entry connector. The pulser circuitry is situated closer to the front of the device, where the BNC connector and power switch, the components that require user interaction, are located. A top-down image of the final device layout is shown below in Figure 25.

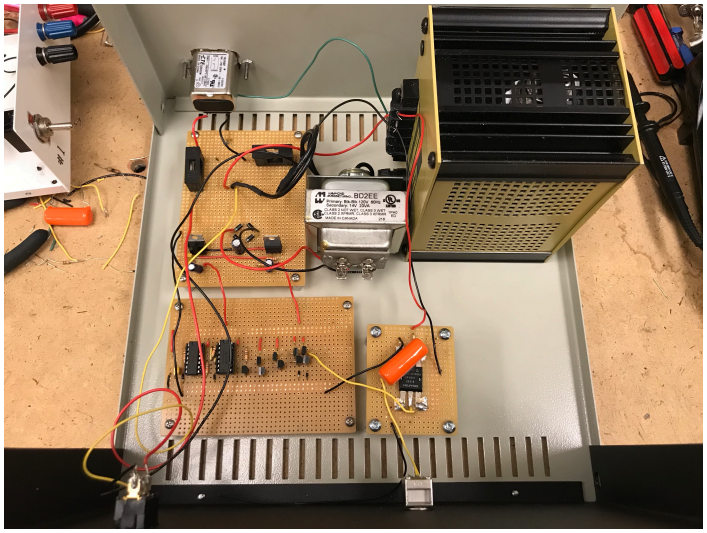


Figure 25: Image of Final Low-Cost Ultrasound Pulser

An image of the front of the device is shown below in Figure 26, and the back of the device is shown below in Figure 27. The most difficult part of this phase of the design was simply drilling all the holes and cutouts necessary to mount each perfboard or provide the user means to interact with the device once the box is sealed.

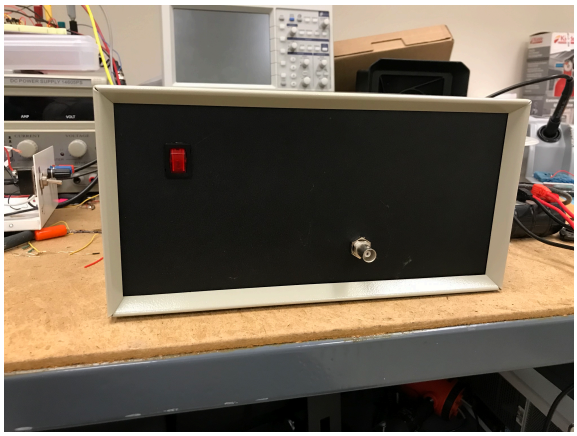


Figure 26: Image of Front of Final Device

Figure 27: Image of Back of Final Device

There are three cutouts for user interaction with the device. The first cutout was made for the power entry connector and allows for a female to male power cord to be connected to the device [21]. The second component cutout is for a BNC connector, which is what allows the user to connect the device to an ultrasound transducer and actually use the device [22]. Finally, the last cutout is for a switch, which allows the user to turn power on and off, meaning that the device can be plugged in without power automatically turning on [23]. This is useful because it provides an extra element of safety—the device will not begin to function until the user desires it to.

7. PERFORMANCE ESTIMATES AND RESULTS

Not every phase of the design process was fully tested, as modifications were made before oscilloscope traces were taken and saved. However, the key phases of the design tested are detailed below, as well as the justification for moving to the next phase of the project.

7.1. Brown and Lockwood's Design Results

The pulser circuit given in Brown and Lockwood's paper was simulated. The simulation schematic and the results of that simulation are shown below in Figures 28 and 29.

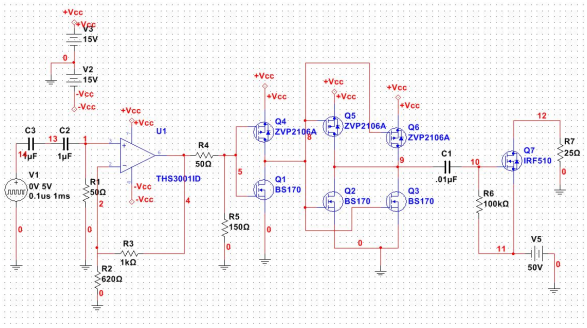


Figure 28: Schematic of Brown and Lockwood's Circuit

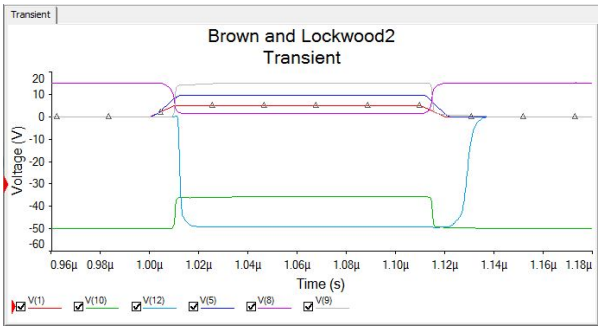


Figure 29: Simulation Results of Brown and Lockwood's Circuit

After the simulation worked reliably, a breadboarded prototype was built, replacing some of the higher-functioning, more expensive components mentioned with components already on hand in the ECBE Department, namely swapping the THS3001 op-amp for the LF356N and the 501N04A power MOSFET for the IRF510. No final output was ever attained from this prototype, but in observing the output of various stages, it was discovered that the width of the output pulse was directly related to the width of the input pulse. As Professor Buma desired a shorter output pulse width, some modification had to be made to the first phase of the pulser circuitry. The correlation between the input pulse width and the output pulse width was observed on the oscilloscope, but not permanently recorded. From this step, the first phase of the pulser circuitry, the pulse generator, was disassembled and a digital logic gate was implemented instead.

7.2. Breadboarded Logic Gate Design Results

The NAND gate pulse generator stage could take a signal of varying duration as its input, so long as the amplitude was around 5 volts. During testing, this stage took a positive 5 volt pulse of 10 μs as its input, and output a positive 5 volt pulse of varying signal width, depending upon the delay resistor, which was 30 kΩ for this testing phase. The output of the pulse generator phase is shown below in Figure 30. The signal out is approximately 6 V, and lasts for 130 ns.

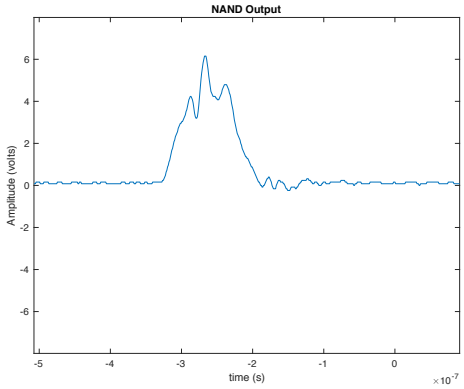


Figure 30: NAND Gate Pulse Generator Output Pulse

During the testing of this design, the need for a level shifter, used to increase the voltage from the 5 volts put out by the NAND gate to the 15 volts required to turn on the P-channel MOSFET, was discovered. This additional phase has already been incorporated into the block diagram of the pulser circuit from Figure 8. Figure 31, below, shows the output of this phase. The voltage of this pulse is approximately -15 V and the duration is 180 ns.

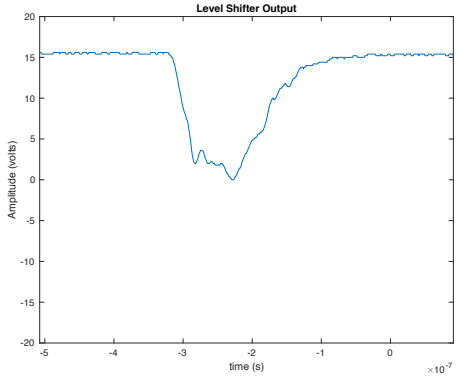


Figure 31: Level Shifter Output Pulse

Each of the two inverting push-pull stages works as desired, inverting the signal fed into it and providing further overall stability. The intermediate output of the two push-pull phases is a positive pulse of approximately 15 V and 140 ns. The final output of the push-pull phases is a negative pulse of approximately -15 V and 140 ns. The outputs of the first and second push-pull stages are shown below in Figures 32 and 33.

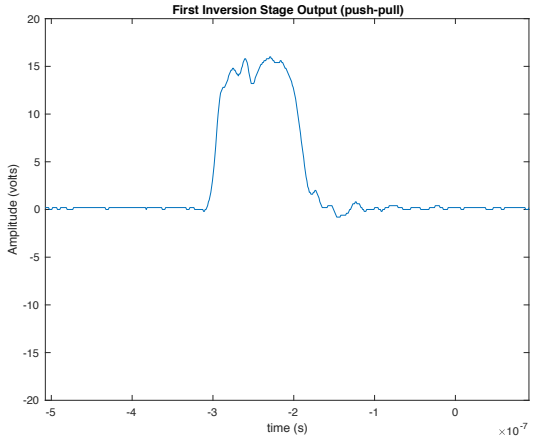


Figure 32: First Inversion Output Pulse

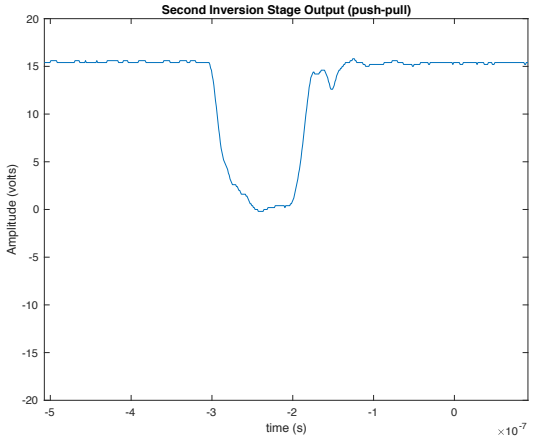


Figure 33: Second Inversion Output Pulse

The current boosting phase inverts the signal one last time so that the input to the power MOSFET is a positive voltage spike. The output of this final inversion stage is shown below in Figure 34, and the signal after it has been passed through the capacitor is shown in Figure 35. The final inversion stage has a positive pulse amplitude of approximately 15 V and 120 ns, and the signal after being passed through the capacitor is identical, but centered around -V_{CC}, -30 V.

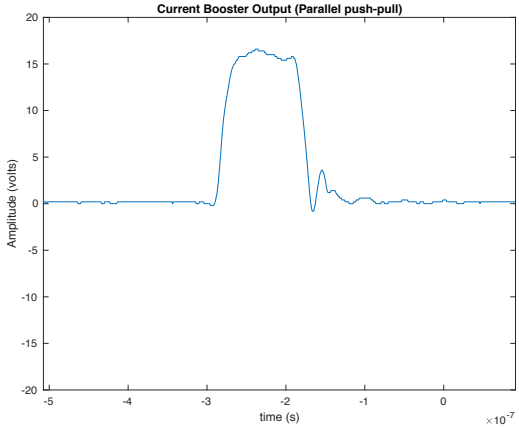


Figure 34: Current Booster Output Pulse

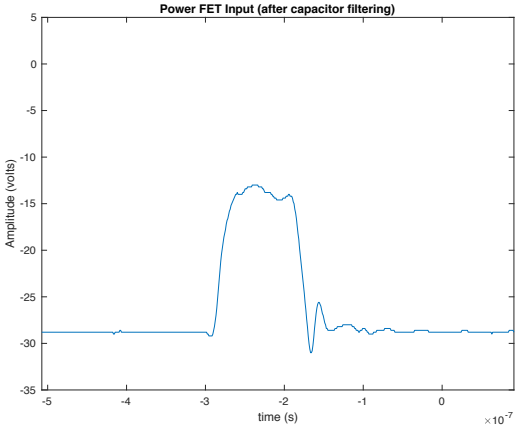


Figure 35: Power MOSEFT Input Pulse

The power MOSFET outputs a negative voltage spike whose highest magnitude is approximately equal to the negative voltage supplied to the source, $-V_{CC}$. This final output is shown below in Figure 36. The pulse width is approximately 120 ns, though it takes an additional 60 ns for the signal to return to 0 V.

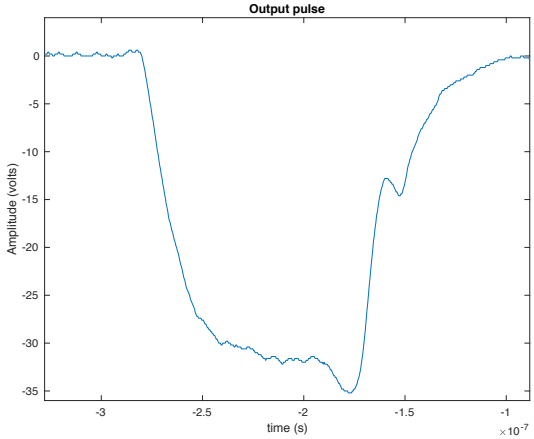


Figure 36: Final MOSEFT Output Pulse

7.3. Soldered Logic Gate Design Results

While attempting to find the appropriate delay resistor for the newly soldered circuit, it was discovered that varying this resistor value would correspondingly vary the output pulse width. An example of this is shown below in Figures 37 and 38. Figure 37 features a pulse of approximately 110 ns, and was taken using a 15 kΩ delay resistor. Figure 38 features a pulse of approximately 330 ns, and was taken using a 100 kΩ delay resistor.

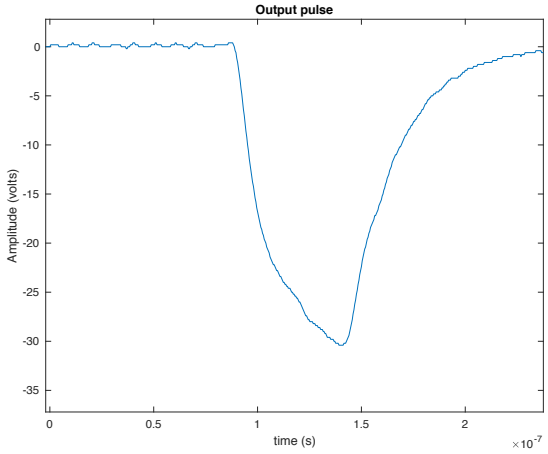


Figure 37: Short Final MOSEFT Output Pulse

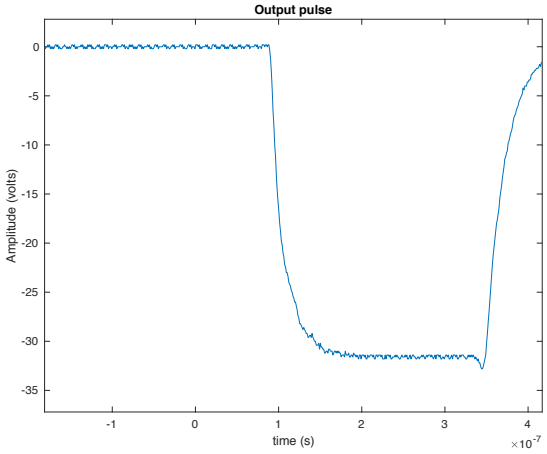


Figure 38: Long Final MOSEFT Output Pulse

The lowest resistor value that provided maximum pulse depth was found to be 15 kΩ. Except for Figure 38, all oscilloscope traces were taken using this 15 kΩ value. The soldered circuit on the whole provided a somewhat faster, more stable signal, but problems of optimization still remained. While the final pulse width was shorter than that of the breadboarded circuit, it was still longer than desired, and not as short as predicted. Part of this behavior could be attributed to the fact that the components used are not the optimal ones decided upon, the inherent delay of the function generator, or the delay associated with the act of taking a scope trace. Further pulse width optimization methods will be explored in the upcoming months.

Measurements were taken at the same places as the breadboarded circuit, and these outputs are shown below in Figures 39-44. The NAND output pulse is about 3 V and 80 ns, while the level shifter is about -15 V and 100 ns.

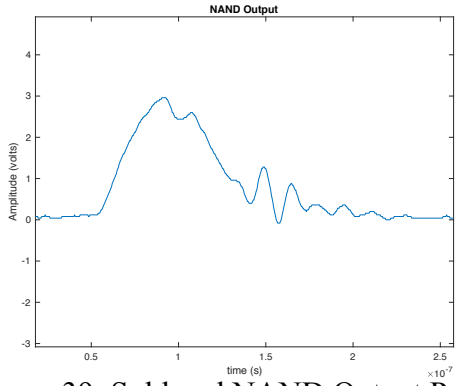


Figure 39: Soldered NAND Output Pulse

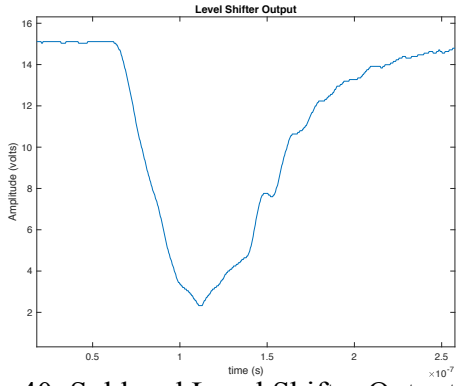


Figure 40: Soldered Level Shifter Output Pulse

The first inversion stage is about 13 V and 90 ns, and the second about -14 V and 90 ns.

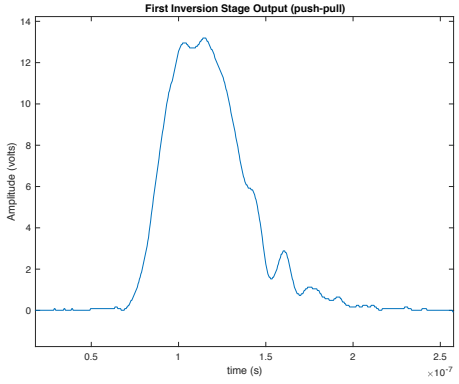


Figure 41: Soldered First Inversion Stage

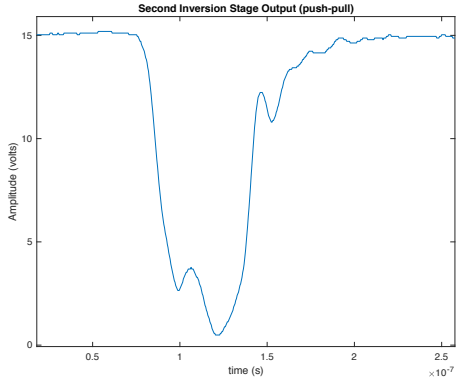


Figure 42: Soldered Second Inversion Stage

The current booster output is approximately 14 V and 90 ns. Again, the signal passed through the capacitor is identical, but it is centered around -29 V instead of 0.

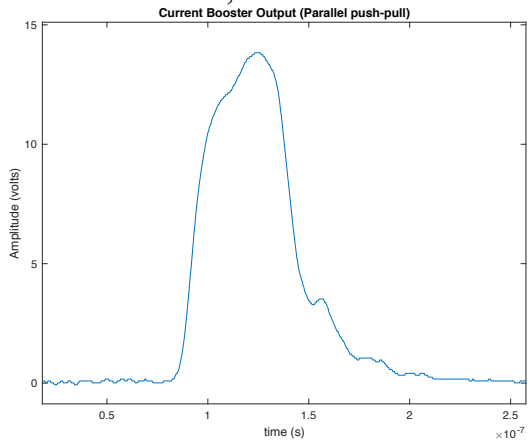


Figure 43: Soldered Current Booster Output

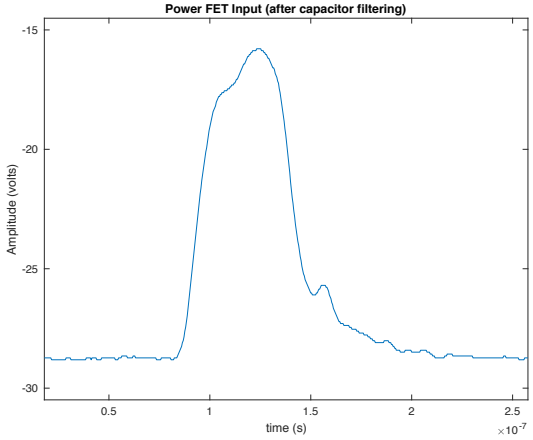


Figure 44: Soldered Power MOSEFT Input

Figure 36 already demonstrates the final output behavior of the soldered pulser circuit. There, the final voltage was approximately -30 V, and the final duration approximately 100 ns, with an additional 50 ns required for the signal to return to 0 V.

One final output test was conducted upon the soldered prototype, using the 15 kΩ delay resistor. $-V_{CC}$ was set at -60 V, and the output was measured, shown below in Figure 45. This high-voltage pulse was approximately - 59 V and 90 ns, though it took an additional 50 ns for the signal to return to 0 V. This high voltage pulse has the same shape and behavior as the lower voltage pulse, with the only difference being the amplitude of the pulse.

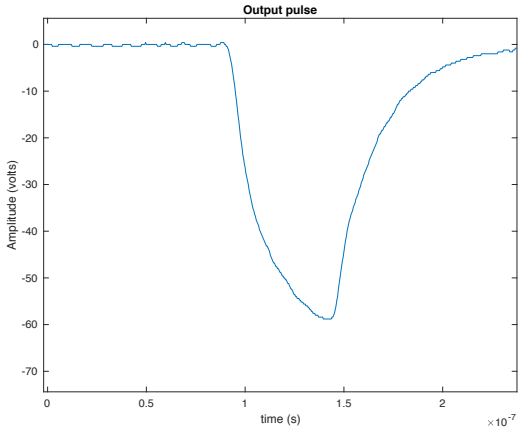


Figure 45: High Voltage Final MOSFET Output Pulse

7.4. Final Design Results

Based upon the value of the delay resistor, the final design performance can vary. Since the intermediate stages' performances are not crucial to the functionality of the device, only the performance of final output, the delay resistor's value was chosen as the lowest value that would still provide the full pulse depth and the shortest pulse width. This resistor value was 10 kΩ in the final design. Because this was the absolute lowest resistor value that could produce the appropriate output, some of the intermediate stages do not reach their full pulse depth. This does not matter, as the output of the current booster stage still provides enough current at a high enough voltage to turn on the gate of the high power MOSFET. A schematic of the overall pulser circuit is shown below in Figure 46.

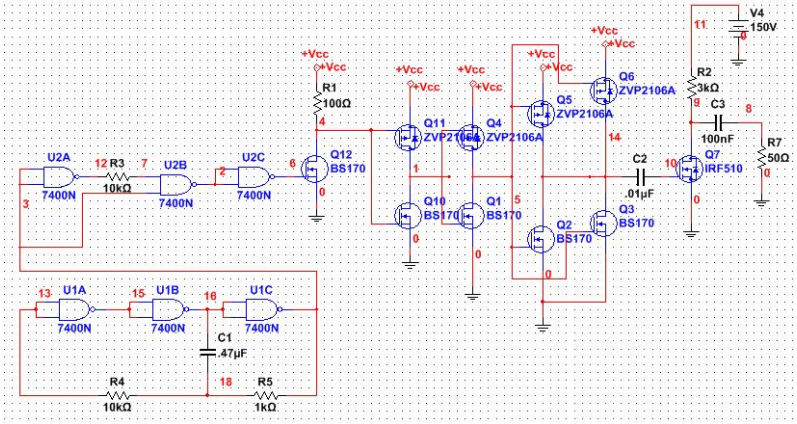


Figure 46: Schematic of Final Pulser Design

This schematic does not include the methods of power delivery implemented in the final device. One other discrepancy between this schematic and the final device is the high power MOSFET used. For the simulations, the IRF 510 was sufficient to verify that the other pulser stages would be able to drive the high power MOSFET, but could not produce more than a 100 V pulse. The final design made use of the 201N09A, which has a maximum drain-source voltage of 200 V, and could therefore produce the appropriate final pulse.

The output of the internal oscillator decided upon, the simple NAND gate oscillator, is shown below in Figure 47. The projected period was 1 kHz, the actual period is approximately 940 Hz.

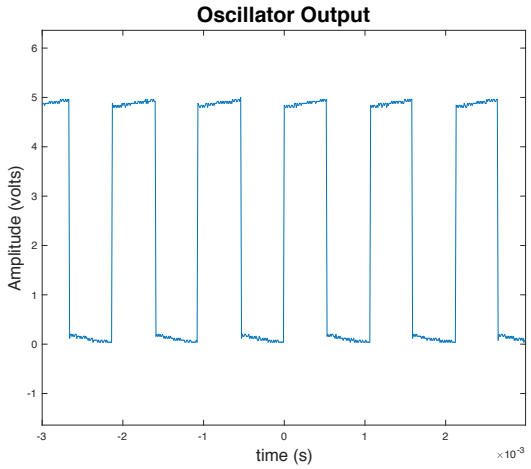


Figure 47: Output of Simple NAND Gate Logic Oscillator

The output of the next stage of the pulser, the low voltage pulse generator, is shown below in Figure 48. This is the stage with the resistor that could affect the final output pulse width, which for this project was decided to be 10 kΩ, the lowest possible value that could still trigger an output. The pulse reaches approximately 3.5 V and lasts approximately 150 ns. The primary peak lasts only 29 ns.

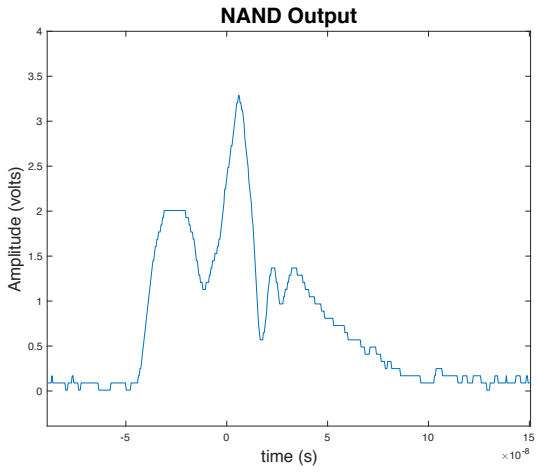


Figure 48: Output of NAND Generated Low Voltage Pulse

After this stage is the level shifter stage, shown below in Figure 49, which uses a BS170 MOSFET to upscale the 5 V output of the previous stage to the 15 V necessary to eventually trigger the final output pulse. The total magnitude of this pulse is approximately 15 V, and the duration is approximately 121 ns.

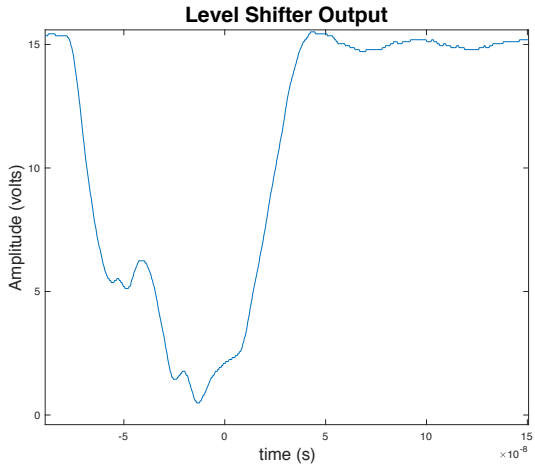


Figure 49: Output of Level Shifter Stage

Following this stage is the current booster stage, which consists of two inverting push-pull stages just before the proper current doubling phase. The output of the first inversion stage, shown below in Figure 50, is approximately 12 V and 134 ns, with the primary part of the pulse lasting 93 ns. The output of the second inversion stage, shown below in Figure 51, is approximately 20 V in peak-to-peak voltage, with a great deal of voltage ripple. The pulse lasted 170 ns, with the primary part of the pulse lasting 66 ns.

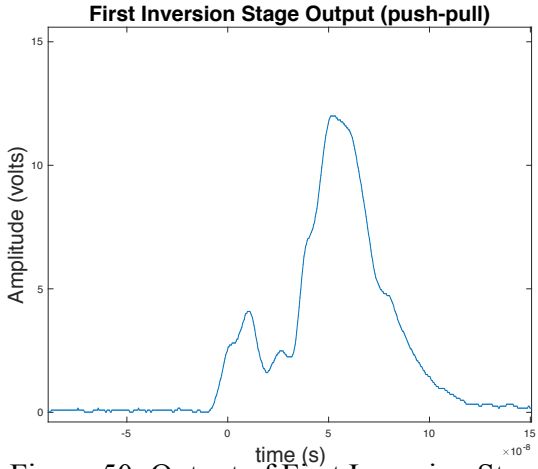


Figure 50: Output of First Inversion Stage

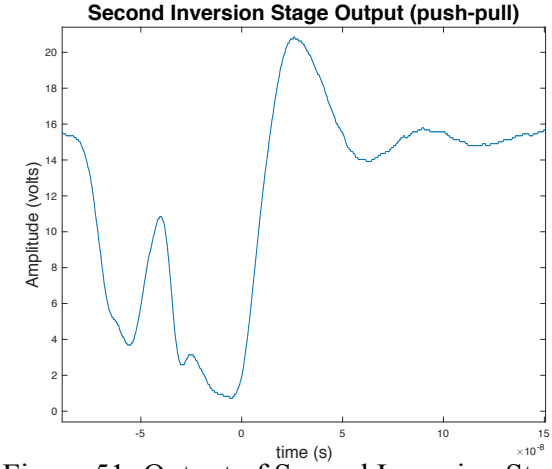


Figure 51: Output of Second Inversion Stage

The proper current booster stage output is shown below in Figure 52. The output is approximately 6.2 V, which does not seem to be enough to drive the final device output, but which will soon prove to be sufficient. The duration of the pulse is approximately 150 ns, with the primary part of the pulse lasting approximately 74 ns.

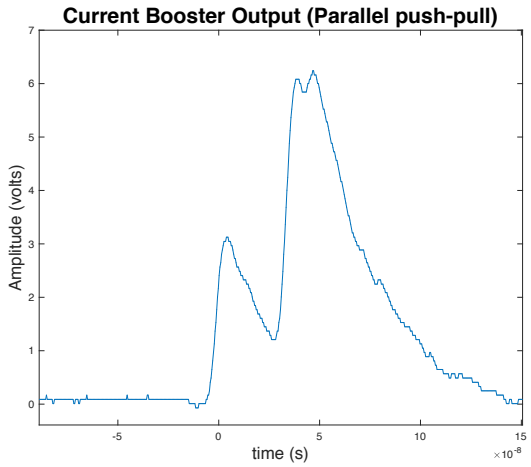


Figure 52: Output of Current Booster Stage

The final output of the pulser circuit, the voltage across the load, is shown below in Figure 53, and the output of the Olympus 5072PR pulser is shown below in Figure 54. The raw output of my device reaches only -135 V, but the total magnitude is closer to 160 V due to voltage ripple. The pulse duration is 120 ns, but the primary part of the pulse lasts only 42 ns.

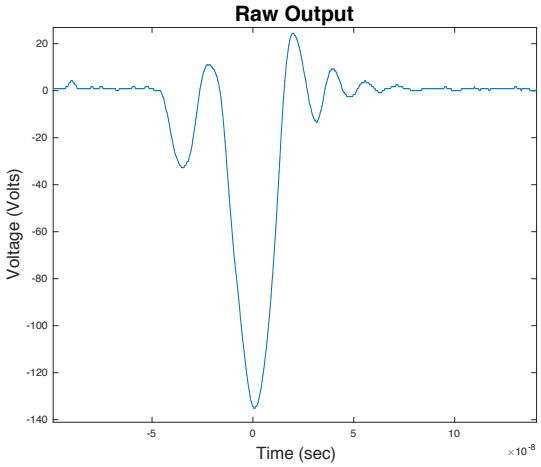


Figure 53: Raw Output of my Pulser

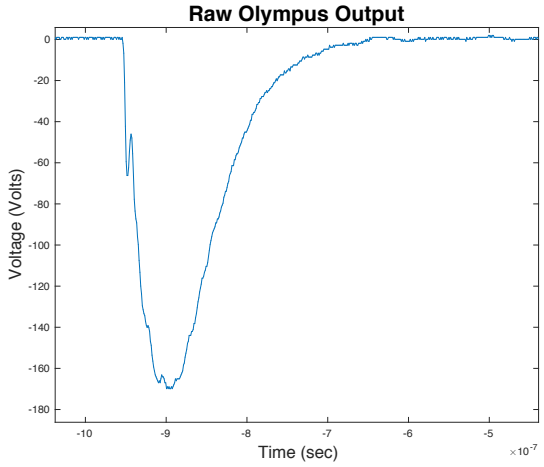


Figure 54: Raw Output of Olympus 5072PR

Comparatively, the raw output of the Olympus 5072PR device reaches a pulse depth of approximately -170 V and lasts for 315 ns, with the majority of the pulse recovery happening within 235 ns. This pulse has significantly less voltage ripple, settling around 0 V nearly instantaneously.

The final output of the device was then connected to an ultrasound transducer in order to determine whether the output pulse could successfully drive an ultrasound transducer. As the device was successful on this front, an image of the received ultrasound output, measured using the Olympus 5072PR, is shown below in Figure 55. This image has little value on its own, but when compared to the ultrasound pulses the Olympus device can output, it can be seen that my device produces comparable results, with the ultrasound pulse's final amplitude falling somewhere between that of the 2nd and 3rd energy settings on the Olympus 5072PR, demonstrated in Figures 56 and 57.

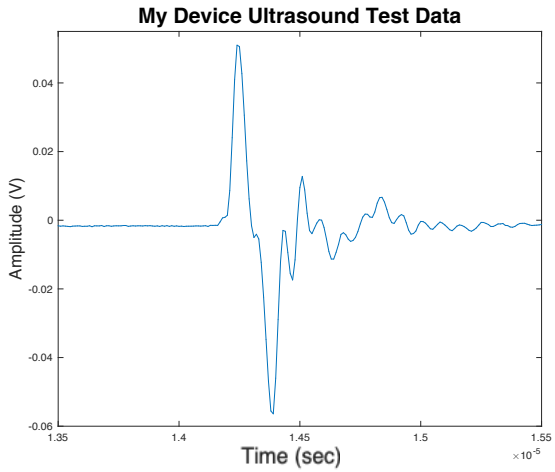


Figure 55: Ultrasound Pulse Generated by my Device

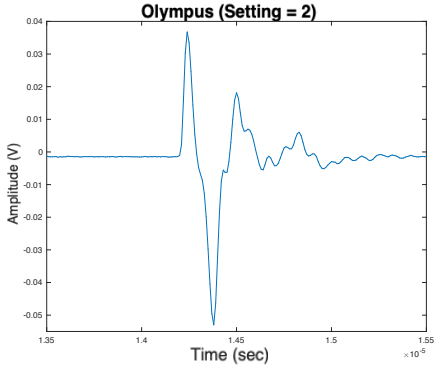


Figure 56: Ultrasound Pulse Generated at Energy Level 2 by Olympus 702PR

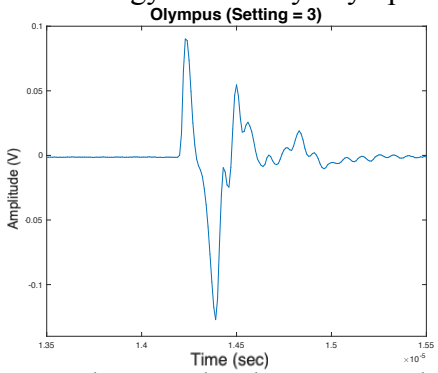


Figure 57: Ultrasound Pulse Generated at Energy Level 3 by Olympus 702PR

When these tests were conducted, a second BNC connector had to be utilized, one that was not connected to the device, and therefore one that was not earth grounded. Because the BNC connector used in the construction of the final device was not isolated, it was earth grounded, meaning that it did not share the same ground as the pulser circuit output. This led to difficulty in taking measurements, so the intermediate solution was to attach a second BNC connector and ensure that the BNC connector was artificially isolated when recording data and running tests.

7.5. Comparison of Preliminary Design to Final Design

In general, the final design behaved quite similarly to initially proposed design. Most of the discrepancies in performance can likely be attributed to the value of the delay resistor. In the preliminary design, a resistor value was chosen that would provide full pulse depth for every stage. For the final design, in consultation with Professor Buma, the value of this delay resistor was selected with only final output in mind, so intermediate performance was not a primary concern. The tests run during the preliminary design phase did not include tests run with the high voltage power supply, and therefore did not include tests involving driving an ultrasound transducer, so that part of the design can not be compared. However, based upon the similarity of the final design to the preliminary design, it is likely that the few changes made in the design did not negatively affect the overall performance of the design.

8. PRODUCTION SCHEDULE

During winter term, several different pieces of the project were worked on simultaneously in order to reach the final production deadline. As the pulser design was being finalized and tested, various methods of generating an internally oscillating pulse were explored, and power delivery strategies were researched. Each of these individual approaches were eventually synthesized into the single final device, constructed during week seven.

8.1. Pulser Production Schedule

The first week of the winter term consisted of refining the existing design through Multisim simulations. At the end of the fall term, it was discovered that Brown and Lockwood's pulser circuit used a high voltage, high current power supply to drive the final stage of the pulser, something that would be far more expensive than the scope of this project demanded and perhaps even the industry device itself. This led to the design choice described in Section 6.2.5, which would not place such a high current demand on the high voltage power supply, instead drawing the current from the high voltage capacitor. As soon as this design was verified in Multisim, it was then prototyped, but at a lower voltage than the 150 volts the Acopian power supply could produce—the 60 volts provided by a standard benchtop power supply.

By week three, this new method of generating the high voltage pulse had been confirmed to provide the expected performance results with the lower voltage output. The pulser now only had to be tested with the 150 volt input and the 201N09A high power MOSFET.

This testing would not commence until weeks six and seven, as attempts were made to verify each individual stage of the circuit before connecting all stages together and powering it using the wall line. When the final high voltage pulse was tested using the 150 volt Acopian

power supply and the 201N09A power MOSFET across a 50 Ω load connected to the breadboard, the circuit behaved as desired, providing the same pulse properties, except that it was reaching the full 150 volt pulse depth.

8.2. Internal Oscillator Production Schedule

During week two, various methods of designing internal oscillation were discussed and considered. The two methods that were prototyped and tested were a 555 timer and a simple NAND gate oscillator. During weeks three and four, two versions of the 555 timer were prototyped and tested—an astable 50% duty cycle square wave generator and an astable pulse generator with a non-50% duty cycle. Neither method behaved as the formulas predicted, so the other internal oscillation method was pursued further during week 5. The simple NAND gate oscillator behaved much more in line with the expected results based upon the calculated values, and therefore was the one chosen for the final application.

8.3. Final Device Production Schedule

Each individual stage was fully tested and prototyped, with the appropriate behavior verified, by the end of week six. The power entry method and overall device housing had been selected and confirmed by the end of week four, so that parts would arrive in time to prototype them before final implementation. Parts arrived during week five, and all preliminary tested ended during week seven. Week seven was when initial testing using all of the final components was conducted and also the very beginning of the construction of the overall device.

The final device was put together during week eight, just before presentations, and verified to work correctly. Tests were performed, both in obtaining simple data traces and in driving an ultrasound transducer. While the final output was not as stable as it had been during

the prototyping phase, the device was able to successfully drive an ultrasound transducer, producing a very similar waveform to that of the industry device, as discussed in section 7.4.

The overall device design process could certainly have been held to a tighter schedule. A primary section of the design phase that could be targeted for improvement is the work that was done over the course of the fall term. If I were to do this project over again, I would spend a lot more time in the fall focused on researching alternate circuit designs for the pulser, running simulations of the potential receiver circuit, and testing ways to implement the desired input adjustments, as I had vague ideas of how to implement them even in the fall. These further research endeavors would have meant far more of the winter term could have been focused on testing and improving the final circuit design, rather than simply using the one design that had been thoroughly prototyped and researched. If I had to redo this project, I would rearrange my schedule so I would have been able to commit more time to only this project.

9. COST ANALYSIS

The overarching requirement of this project was cost, as it was billed as a low-cost alternative to the industry device. Therefore, while it is not a technical requirement, cost was a primary restriction of this project. The most expensive component was the Acopian B150GT10 high voltage power supply, at $245. The device housing cost $56.53. Though it was not a part of the main circuit, the BD2EE power transformer was the next most expensive part, at $19.15 and was required in order to power the power MOSFETs for the push-pull level shifter and current booster stages. After that, the next most expensive part, was the high power MOSFET, at $14.21. The next part of significant cost was the high voltage capacitor, at $3.10. The cost of these primary components totals $337.99, which is slightly less than one fifth as high as the approximately $2,000 cost of the industry device. Excluding the high voltage power supply, the total device cost is $92.99. Excluding the cost of the device housing and assuming that the correct voltage values can be delivered without the transformer, the cost of the components necessary to produce the desired functionality is $17.31. All other components were of far lower cost; the breakdown of specific components by cost is shown below in Table 1.

Table 1: Device Components Broken Down by Cost

Quantity	Item	Cost
1	Acopian Power Supply Model B150GT10	$245.00
1	201N09A Fast Power MOSFET	$14.21
1	715P10452LD3 High Voltage Capacitor	$3.10
5	BS170 Power MOSFET	*
4	VP2016 Power MOSFET	*
2	SN74HC00N Quad NAND Gate Chip	*
1	LM317 Voltage Regulator	*
1	LM7805C Voltage Regulator	*

4	1N4002 Diode	*
1	Hammond B2DEE Power Transformer	$19.15
1	Hammond 1426Q Device Housing	$56.53
2	4628 Fuse Holder and 4628C Fuse Cover	$0.92
1	Pack of 5 250mA Slow Blow Fuses	$7.99
1	Philmore Miniature Lighted Rocker Switch	$4.99
Varied	Various Standard Resistors and Capacitors	*
Varied	Perfboards	*
	Total	$352.81

Components whose cost is denoted by an asterisk in Table 1 were readily available within the ECBE department and therefore did not cost anything to obtain. While various components that allow the device to function increase its cost greatly, the components that generate the high voltage pulse that will eventually drive an ultrasound transducer are quire affordable, at less than $20 for the components directly related to the generation of the pulse (meaning the high power MOSFET and the high voltage capacitor) that had to be purchased. Brown and Lockwood claimed that their design would cost less than $50, and this design, counting only the components used in the overall pulser circuit should also be less than $50, but can be used with far less powerful power supplies than theirs. Even when the cost of absolutely every component used in the construction of the device is tallied, it stills costs less than $400, which is the Student Research Grant maximum, meaning this project is well within the scope of a student project and can be replicated at a comparably low cost to the industry device.

10. USER'S MANUAL

10.1. Device Operation

In order to drive an ultrasound transducer, the device has three very simple steps. An external ultrasound receiver will be needed to collect data, however.

1. Plug the device into the wall using a standard female to male three-prong power cable.
2. Connect the ultrasound transducer to the BNC output on the front of the device.
3. Flip the red switch to turn on power. (If power is on, the switch will light up).

The device will then output a -150 V pulse for a duration of approximately 42 ns at a persistent 1 kHz repetition rate until the device is turned off again. This should be sufficient to drive an Olympus V384 3.50 MHz ultrasound transducer.

10.2. Device Troubleshooting

If the device is not performing as expected, the first thing to do is disconnect from the wall line before attempting any initial troubleshooting to ensure user safety. From there, check solder connections to ensure that all components are correctly connected, both to the appropriate other components and to power and ground. After verifying connections, plug device in and test again. If device is still not providing desired results, measure voltage outputs to ensure that correct voltage levels are being delivered to components, but be especially careful of exposed high voltage wires. If device is receiving appropriate voltage and still not behaving appropriately, check high power MOSFET for desired behavior, then begin checking signal at various stages. The points that should be measured most closely are the internal oscillator output, the low voltage pulse generator output, the level shifter output, and the output of each push-pull stage, as well as the high power MOSFET that was examined during the previous troubleshooting phase.

If all stages are producing desired results and the device still does not behave as expected, re-solder the final power MOSFET stage. After all previous steps have been taken, if the device still does not behave as expected, it is likely best to rebuild the whole design from scratch.

11. DISCUSSION, CONCLUSIONS, AND RECOMMENDATIONS

11.1. Discussion

In order for this project to have been considered successful, it had to meet one primary, overarching goal: it had to be able to successfully drive an ultrasound transducer at a significantly lower cost than that of the industry device Professor Buma uses. Before connecting the device output to an ultrasound transducer, there were several specifications that needed to be met that would suggest that the pulser was working as expected. The ultrasound transducer requires a very short, very negative voltage spike in order to produce ultrasound waves. This pulse also needed a way to be triggered, so that the device could successfully output the pulse.

I approached this project initially by simulating the design of Brown and Lockwood [2]. When I was unable to get the prototyped version of their design to function as laid out in their paper, I began to make some changes, under the guidance of Professor Buma. The first major change was the use of digital logic to create the initial pulse that would be carried through the circuit instead of the op-amp they used. Much of the fall term then involved getting a working prototype of this circuit design, a goal that was not achieved until very late in the term, perhaps week eight or nine. Toward the end of the fall, the two most important components were ordered: the high voltage power supply and the high power MOSFET.

The first part of the winter term involved further refinement of this circuit design. One large issue with the Brown and Lockwood circuit was that the high power MOSFET was connected directly to the high voltage, and therefore drawing a great deal of current directly from the high voltage power supply. While this is not an inherent problem, most low-cost high voltage power supplies cannot produce the current necessary to drive the high power MOSFET, meaning

that an alternate method of current delivery had to be implemented. This alternate method ended up being a high voltage capacitor with a very high dV/dt, so that the component providing the high current would not be the power supply but instead the capacitor. The first quarter of the winter term was dedicated to refining this part of the circuit.

The second quarter of the winter term focused on designing and selecting the internal oscillation method. Several options were considered and eventually eliminated, before finally deciding upon the NAND gate oscillator. The second half of the winter term then focused upon final construction and testing of the device. Part of the final construction included researching various methods of power delivery and ways to ensure the device was safe. Lastly, the device was tested and final performance was recorded.

Though not every design specification was met, the final device designed was still able to successfully drive an ultrasound transducer and even produced similar final ultrasound behavior as the industry device. There is a great deal of future work to be done in modifying parts of the circuit to provide the desired adjustability and increased performance, but overall the device was able to meet the fundamental goal of the project—to drive an ultrasound pulser at a fairly low cost (as compared to the industry device).

The biggest takeaway from this project was the importance of time management and self motivation. Something I did not realize during the initial stages of this project was just how little time there actually was to research the topic and the components before I needed to begin designing a prototype and suggesting alternatives. As each individual stage of the pulser circuit was designed (or refined), I should hovels been researching ways to alter those stages to meet the original goals of the project. Looking back now, many of the goals related to higher functionality

could have been easily implemented with just another week or two of research and work. As the term wore on, there were fewer and fewer days in which I could accomplish things, and fewer and fewer days in which to produce results. If I were to do this project all over again, I would have spent far more time researching components and learning about the topic before even beginning the project. Another seemingly silly thing I would have done is enrolled in fewer courses, as attempting two senior projects (one being this project) on top of a full course load definitely detracted from the time and quality of work I was able to put into this project during the fall term.

The most important lesson I learned from this project was that a seemingly simple design can in fact take hours to test, prototype, and troubleshoot. Often, I would go to work on the device, thinking I would be able to make a few small adjustments in order to achieve whatever I was trying to do, say for example design a stable internal oscillation method. This actually meant I had to decide upon component values, simulate those values, prototype the circuit, compare it to the simulation, and attempt to understand why the prototype did not (or did) behave as expected. Solving this last part of the problem often involved hours of checking connections and verifying component values. This is a valuable lesson moving forward as I will surely be faced with problems in the future that will not have a simple solution or a one-day fix. After working on this project for so long, I understand the importance of not rushing a design and really spending the time and effort to understand why each separate component is necessary, as well as why the signal or device behaves in the way it does. This deep level of understanding allows for far easier troubleshooting, as it is far easier to solve a problem if I understand what could be causing that problem.

11.2. Conclusions

The biggest requirements of this project had simply todo with the ability to output a basic pulse capable of driving an ultrasound transducer. This meant the output pulse had to be deeply negative, able to reach full pulse depth, and shorter than 100 ns. The pulse had to repeatedly self-trigger at approximately 1 kHz. All other project goals were either related to higher functionality or to the receiver circuitry, two overall goals that were eventually cut due to time constraints.

For this project, the value of the negative voltage spike was determined by the value of the high voltage power supply, which was 150 V. The final voltage had to reach -150 V, but had a higher voltage power supply been chosen, the device should have been able to output that voltage as well. The final output pulse had to reach the total expected pulse depth in order to be considered functional. The device was able to produce a voltage spike of approximately -151 V, which was likely based upon some minimal voltage ripple and rounding error. The output voltage range fell within acceptable limits.

The duration of the pulse was also a primary concern, as it would not be able to drive the ultrasound transducer if it was too long. The pulse had to be less than 100 ns. The actual final pulse width was 60 ns, meaning that the pulse width too fell within an acceptable range. The initially desired pulse width was 20 ns; however, so improvements definitely could be made.

The internal oscillator was necessary so the device could simply be plugged in and connected to an ultrasound transducer. This meant that a repetition rate had to be decided upon. 1 kHz was agreed upon as a value that would provide basic functionality, and the internal oscillator design was able to provide a repetition rate of 940 Hz. With further fine-tuning of resistor and capacitor values, this repetition rate likely could have been made exactly 1 kHz. Regardless, the

internal oscillator provided the means for the device to trigger itself, meaning it required no other devices in order to produce the pulse necessary to drive an ultrasound transducer.

Some other goals involved making the device higher functioning (adjustable pulse width, variable repetition rate, and external trigger), but were not necessary in order to simply drive an ultrasound transducer. These adjustments would have allowed for finer tuning of the signal and better overall performance, but their absence does not hinder the device's ability to meet the main goal. So, although not every goal was met, and receiver circuitry was not designed, the pulser goal of the project was met, as the designed device was able to drive an ultrasound pulser.

11.3. Recommendations

Several recommendations can be made to improve device performance and meet original design specifications. Many of these recommendations have been planned out but not implemented, although some remain hypothetical only.

Firstly, in order to achieve the variable repetition rate originally desired, one simply has to change the values of the resistors used in the internal oscillation circuit, shown in Figure 18. R1 should always be ten times as large as R2, so resistor values for each desired repetition rate should be decided upon using Equation 3, from Section 6.2.1. After choosing 4-5 different repetition rates, a simple rotary switch can be used to switch between the appropriate resistor pairs for those repetition rates.

Similarly, in order to achieve a variable pulse width, the value of the delay resistor can be changed to make the pulse width wider. One can experimentally determine the appropriate delay resistor value for any given pulse width, and can select 4-5 desired pulse widths. Again, a simple rotary switch can be used to switch between the different delay resistors in order to achieve a

variable pulse width. For this stage, one should re-confirm that the delay resistor provides the expected pulse width, as the switch may add resistance that could affect the final pulse width.

The next suggestion has to do with the external trigger. This would consist of either a method to entirely bypass the internal oscillator and use an external function generator, or a method to turn the internal oscillator on and off, something that would already be included in the bypass method. A simple single pole, single throw, or double pole, single throw switch connected to the internal oscillator stage input would allow for the breaking of that circuit and therefore the bypassing of that stage. Adding a second BNC connector, connected to the input of the low voltage pulse generator stage, would allow for external signals to be routed into the device. By implementing these two components, an external trigger could easily be introduced to the device.

Another original requirement that was not met was the total receiver circuitry design and implementation. The requirements for the receiver were detailed extensively in Section 3.2, and potential designs were discussed in Sections 4.1.2 and 5.2. These requirements and preliminary designs should serve as the basis for any future work done on receiver design for this application.

The design could be implemented on a PCB (once all the improvements discussed above have been made), which should provide further signal stability and increased performance. This would also make the overall device safer, as there would be far less exposed wires carrying high voltages throughout the device.

One final recommendation would be to test various other high speed power MOSFETs. The 201N09A has a high drain-source voltage and very fast turn-on time, but it is plausible that other high power MOSFETs might provide similar results, even if they have slightly slower turn-on times, for example the IRF620, which has a turn-on time of 7.2 ns [24].

12. REFERENCES

[1] Olympus, “Manually Controlled Pulser-Receivers,” 5072PR datasheet, 2009.

[2] J. A. Brown and G. R. Lockwood, *A Low-Cost, High-Performance Pulse Generator for Ultrasound Imaging,* IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control., vol. 49, no. 6, June 2002, pp. 848-851.

[3] J. K. Poulsen, *Low Loss Wideband Protection Circuit for High Frequency Ultrasound,* IEEE Ultrasonics Symposium, 1999, pp. 823-826.

[4] L. Svilainis and V. Dumbrava, *Design of a Low Noise Preamplifier for Ultrasonic Transducer*, Ultragarsas, vol. 55, no. 2, November 2005, pp. 28-32.

[5] Texas Instruments, “420-MHz High-Speed Current-Feedback Amplifier,” THS3001 datasheet, July 1998 [Revised September 2009].

[6] Texas Instruments, “LFx5xJFETInput Operational Amplifiers,” LF356N datasheet, May 2000 [Revised November 2015].

[7] IXYS RF, “DE150-501N04A RF Power MOSFET,” 501N04A datasheet, 2009.

[8] Intersil, “5.6A, 100V, 0.540 Ohm, N-Channel Power MOSFET,” IRF510 datasheet, November 1999.

[9] Fairchild Semiconductor, “BS170 / MMBF170 N-Channel Enhancement Mode Field Effect Transistor,” BS170 datasheet, March 2010.

[10] Supertex, Inc. “N-Channel Enhancement-Mode Vertical DMOS FETs,” VN2106 datasheet, 2008.

[11] Supertex, Inc. “P-Channel Enhancement-Mode Vertical DMOS FET,” VP2106 datasheet, 2009.

[12] Texas Instruments, “SNx4HC00 Quadruple 2-Input Positive-NAND Gates,” SN74HC00N datasheet, December 1982, [Revised July 2016].

[13] IXYS RF, “DE150-201N09A RF Power MOSFET,” 201N09A datasheet, 2012.

[14] Acopian, “Gold Box UNREGULATED AC-DC single output & wide adjust output,” U400Y20 datasheet.

[15] Hamamatsu, “Compact High Voltage Power Supply C4900 Series,” C4900 datasheet, June 2012.

[16] Acopian, “Gold Box LINEAR REGULATED AC-DC single output Series A & B,” B150GT10 datasheet.

[17] Electronics Tutorials, “555 Oscillator Tutorial,” [online]. Available: https://www.electronics-tutorials.ws/waveforms/555_oscillator.html. [Accessed: 2-14-2019]

[18] Electronics Tutorials, “Stable NAND Gate Waveform Generator,” [online]. Available: https://www.electronics-tutorials.ws/waveforms/generators.html. [Accessed: 2-14-2019]

[19] Cornell Dubilier Electronics, “Type 715P, Orange Drop®, Polypropylene Film/Foil Capacitors,” 715P10452LD3 datasheet, Accessed 1-21-2019.

[20] Hammond Manufacturing, “Class 2 Energy Limiting Small Box Mount,” BD2EE datasheet, 2018.

[21] TE Connectivity, “SRB Series,” 15SRBP datasheet, June 2011.

[22] Molex, “BNC Jack RA Bulkhead Diecast 50 Ohm BNC-J/PCB,” SDA-0731385033 datasheet, April 2006.

[23] Philmore, “Master Catalog,” Miniature Lighted Rocker Switches datasheet, 2012.

[24] Vishay Siliconx, “IRF620, SiHF620 Power MOSFET,” IRF620 datasheet, March 2011.

13. APPENDICES

The following pages feature appendices with the following information:

- **Appendix A:** Original SRG proposal (submitted Fall ’18)
- **Appendix B:** Notice of SRG Funding
- **Appendix C:** ECE-498 Poster from 11/1 Poster Session Week 9
- **Appendix D**: ECE-499 Slides from 3/2 Presentation Session Week 8 Winter Term
- **Appendix E:** ECE-499 Poster from 3/11 Poster/Demo Session Week 10 Winter Term

Appendix A: Original SRG Proposal (Submitted Fall 2018)

Project Proposal
Andrea Huey

Introduction: Ultrasound imaging is a vital medical technology, as it allows professionals to get a closer look at the inside of what they are studying without actually having to open the person or object they are attempting to observe. While this variety allows people the ability to choose exactly what they want in a machine, many industry machines are designed with a great deal of adjustable features, and therefore cost a great deal of money. The primary goal of this project is to design a low-cost pulser/receiver. Some additional functionality is desired, and will be designed into the project, but the current plan is to have the main phase of the design completed by the end of fall term. The first half of winter term will entail adding optional features to the device, and the second half ensuring that the overall device is functional and presentable.

Proposed project: As mentioned above, this project involves creating a low-cost alternative to the over a thousand dollar machine Professor Buma has (and uses). The low cost aspect also means that should Professor Buma need more than one pulser, he does not have to purchase another expensive machine, rather; he can use another, simpler device. Designing this device will also allow me to work with a topic not covered in depth through any course here at Union. The majority of the project time will be spent working with the individual circuit elements, trying to build a functional prototype, but the desired finished project should be constructed on a Printed Circuit Board (PCB) and mounted in a metal enclosure, with appropriate BNC connectors to allow the device to be connected to coaxial cables and used just like the more expensive machine it is based on. An image of the original machine is shown below for reference, but my device will likely not look identical. Additionally, a rough sketch of the device in use is shown.

Figure 1: Image of Professor Buma's device

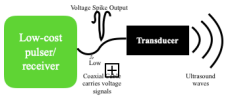


Figure 2: Sketch of key device stages

Design Requirements:
Output Requirements: The pulser shall produce a negative voltage spike around 180 volts (V) or greater, for 20 nanoseconds or less. A greater voltage spike, around 350 V, is more desirable, but 180 volts is a starting baseline. The repetition rate shall begin at 1 kilohertz (kHz), but can (and should) eventually be adjusted to go as high as 20 kHz. 5-10 kHz would be considered a more typical goal. The unit should also have two different trigger options; an internal trigger (that would keep time and self-trigger) and an external trigger (that would operate on a 0-5 volt logic scale and trigger due to an input signal to the device). Adjustability with regards to both the repetition rate and the triggers are longer term goals, but is desired.

Input Requirements: For initial testing, the load will be assumed to be 50 ohms. The receiver should be capable of measuring the pulse echo. One cable will be used both to transmit and receive, and as such, needs to be able to route a very high voltage signal and a very low voltage signal with no data loss at either extreme. The receiver circuitry would also need to be protected against the very high voltage pulse by using a duplexer and limiting diodes.

Cost Requirements: As the project is meant to be a cheaper alternative to Professor Buma's approximately $2,000 machine, the economic cost of this project is definitely a constraint. The design proposed in Brown and Lockwood's paper costs around $50, so the final circuit design, which would have more functionality than their proposed design, and include additional elements, would ideally be under $100, discounting the costs of the high voltage supply, the PCB, and the mounting hardware. More discussion of cost will be featured in the Budget section.

Electrical/Safety Requirements: The pulser/receiver shall run off the 120 volt wall line, and will be designed with those limitations in mind. It likely will not be used to take measurements on living beings, but it should be safe enough for such an eventuality. Because of the very high voltage, the system shall be designed with careful attention paid to the current running through components and the amount of power dissipated.

Size Requirements: The original machine is approximately 7 inches wide, 3.5 inches tall, and 9.1 inches deep, so my device should be no larger than those dimensions. Since this device will be a low-cost version, it should be even smaller than the more expensive machine. I do not yet have exact dimensions, as they will depend on the final circuit design and the size of the PCB and other components.

Design Approach: Much of the aesthetic elements of the project will be implemented during the winter term, after various sub-functions are confirmed to be working as expected. The goal for the end of the term is to have the pulser and receiver elements of the device functioning, and a preliminary design for the final device housing should be implemented. A high level block diagram of the key stages is shown below.

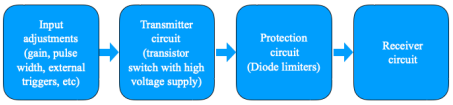


Figure 3: Overall Model of the Pulser/Receiver

The pulser will initially be tested alone. In order to do this, an oscilloscope probe can be used to measure the system output and display it on the oscilloscope. The output will be measured with and without a 50 Ω load. The voltage amplitude, duration of the pulse, and any pulse ringing will be the main aspects of the signal to observe.

The receiver will also be tested by itself before it is implemented with the pulser. A function generator will be used to model the input signal. Again, a scope probe will be used to measure the output of the receiver. In this case, the amplifier gain, frequency response, and noise will be the observed parts of the signal.

When both the pulser and receiver are tested together, the output (of the pulser)/input (of the receiver) cable will be connected to an ultrasound transducer. The transducer will then be placed in front of an acoustically reflective device, and a pulse will be sent. The final output of the receiver will be measured using an oscilloscope. Here, it is the peak frequency and bandwidth of the received pulse that will be measured.

These methods can be used to test each step of the device individually, but will also be used in the future to test the device when additional features are added. Assuming that a successful pulser/receiver is designed, the final result of those tests will be used as a benchmark for the device's future functionality, with appropriate scaling.

Anticipated Outcomes: The final device should behave comparably to the one Professor Buma is currently using. It should, at minimum, be able to send a very high voltage pulse (on the order of a hundred volts) to the ultrasound transducer and receive the very low voltage pulse (on the order of millivolts) sent back through the transducer. Additionally, some front-end adjustments will be implemented. These requirements include, but are not limited to, adjustable gain, adjustable pulse width, and adjustable gain, all of which should be able to be implemented with fairly simple circuit components. These components include variable resistors or capacitors, as well as regular resistors, capacitors, inductors, and other simple circuit components. Though the device may not be as finely tuned or accurate as the one Professor Buma currently uses, it should be able to be used for a rough estimation of the imaging work he is trying to accomplish.

Reason(s) Funding is Necessary: Funding is necessary for this project because I will need to be able to purchase key components, such as a high voltage supply, PCB materials, and mounting materials in order to successfully create and test the ultrasound pulser/receiver.

References:
[1] J. A. Brown and G. R. Lockwood, *A Low-Cost, High-Performance Pulse Generator for Ultrasound Imaging,* IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control., vol. 49, no. 6, June 2002.

[2] Olympus, "Manually Controlled Pulser- Receivers," 5072PR datasheet, 2009.

[3] J. K. Poulsen, *Low Loss Wideband Protection Circuit for High Frequency Ultrasound,* IEEE Ultrasonics Symposium, 1999.

Budget Breakdown: The components necessary to complete the device are broken down in the table below. The total amount requested is $399, with $362 going toward component purchase and $37 for shipping costs. The most expensive component is the high voltage supply, which is also the most necessary, due to the fact that the project features high voltage spikes. Many standard electrical components, such as resistors, transistors, and op-amps, can be found in the ECBE department, and so their cost is not included in the budget breakdown.

Table 1: Detailed Budget Breakdown

Item	Justification	Cost
Acopian Power Supply Model U400Y20	This high-voltage power supply can produce up to 400 volts. 400 volts is necessary to create a buffer for the maximum 350 volts Brown and Lockwood's circuit was designed for, though most of the testing will be conducted at a lower voltage. When using high voltage, care will be taken to ensure user safety.	$250
THS3001 Operational Amplifier	420 MHz current-feedback amplifier, used as a high input impedance line driver	*
3 VN2106 MOSFETs and 3 VP1304 MOSFETs	These MOSFETs are paired together (1 P-Type and 1 N-Type) to act as a push-pull switch.	*
501N04 Fast Power MOSFET	Used as a high power switch to turn the circuit on or off.	$27
2 50 Ω Resistors	Component in pulser circuit	*
150 Ω Resistor	Component in pulser circuit	*
1k Ω Resistor	Component in pulser circuit	*
25 Ω Resistor	Component in pulser circuit	*
100k Ω Resistor	Component in pulser circuit	*
620 Ω Resistor	Component in pulser circuit	*
2 1.0 µF Capacitor	Component in pulser circuit	*
0.01 µF Capacitor	Component in pulser circuit	*
2 BNC Connectors	Necessary to input/output voltage pulse and resultant signal, and to input external trigger	$11
Custom PCB Fabrication	Necessary for the final device to be neatly organized	$32
Mounting Hardware	Includes mounting enclosure, small metal sheets, screws, spacers, and washers	$42
Shipping Costs	Must pay for shipping for some specialty websites/companies	$37

* These components will be paid for by/are freely available in the ECBE department.

Appendix B: Notice of SRG Funding

Dear Andrea Huey,

It is with pleasure that I am writing to inform you that the Student Research Grant Committee has approved a student research grant in the amount of $399.00 to enable you to carry out the project outlined on your application. ***Please read the following comments and directions carefully:***

The SRG Committee recommends funding of $399 for the purchase of materials related to your project. Please work directly with Lisa Galeo in the ECBE department to make the necessary purchases.

This grant is being made out of funds budgeted for the academic year 2018-2019. You may draw upon your SRG account through early May 2019 – **all spending must be completed by Friday, May 10, 2019 and receipts must be turned in by Tuesday, May 14, 2019.** You will be expected to spend these funds in general accord with the budget approved for your project.

Guidelines for spending your SRG funds can be found at:
http://muse.union.edu/undergraduate-research/student-research-grant-applications/

The Committee extends its best wishes for a successful project.

Sincerely,

Chad Orzel
Director of Undergraduate Research
Chair, SRG Committee

Cc: Prof. Chad Orzel (via separate email)
Advisor: Prof. Takashi Buma (via separate email)
Dept AA (for Reimbursements): Lisa Galeo (via separate email)

~~~
~~~

Ruth A. Cotter
Assistant to the Dean of Studies
Union College
F.W. Olin Center 210C
Schenectady, NY 12308
(518) 388-6234

Appendix C: ECE-498 Poster from 11/1 Poster Session Week 9 Fall Term

Senior Project – Electrical Engineering and English Double Major – 2019

Designing a Low-Cost Ultrasound Pulser/Receiver

Andrea Huey
Advisor – Prof. Takashi Buma

Introduction:

- Ultrasound imaging is an incredibly powerful technology that grants the ability to see inside a patient or subject without cutting them open
- Ultrasound pulse transmitted by applying high voltage pulse to an ultrasound transducer
- Same transducer detects echoes, which are amplified to obtain data and reconstruct an image
- Commercial pulser/receivers can cost several thousand dollars
- Professor Buma needs a low-cost alternative so he can conduct experiments with multiple ultrasound transducers

Design Requirements:

- Pulser shall produce a -180 V spike, but should ultimately reach -350 V
- Duration of voltage spike should be <20 ns
- Initial repetition rate of 1 kHz, eventually shall be adjustable to 20 kHz
  - 5-10 kHz considered more attainable goal
- 2 different trigger options desired
  - Internal trigger that keeps time and self-triggers
  - Input trigger that operates on 0-5V logic scale
- Long term goals include repetition rate and trigger adjustability
- Most obvious requirement is cost since this is a a low-cost alternative

Preliminary Results:

- Designed and tested pulser circuit, working from preliminary circuit given in Jeremy A. Brown and Geoffrey R. Lockwood's paper

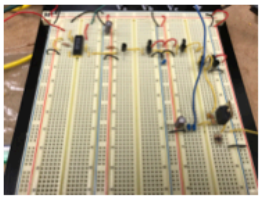


Figure 4: Breadboarded Pulser Circuit

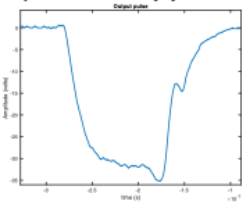


Figure 5: Final Circuit Output

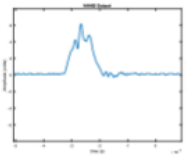


Figure 6: NAND Output

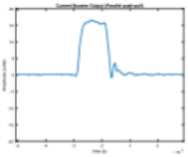


Figure 7: Current Booster Output

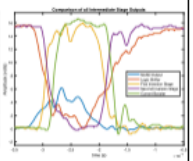


Figure 8: Multi Signal Comparison

- Final output pulse width is shorter than input stages, but is not yet at the desired pulse width of 20 nanoseconds
- Each stage has the general desired response, ignoring ripples
- Next step is soldering components and testing if that decreases pulse width and excess ringing/ripple
- Once pulser works as desired, begin designing/testing receiver

Preliminary Design:

- The pulser consists of four primary stages

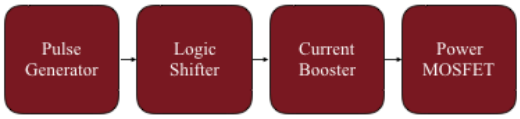


Figure 1: Block Diagram of Pulser Circuit

- Pulse Generator takes advantage of the inherent propagation delay in digital logic (NAND) to create a short pulse (~200 ns) from high input
  - In theory, this delay should be enough to produce the desired behavior, but a resistor was needed to further slow down the response
- Logic Shifter takes the final NAND output stage and the input value from +5V to +15V output in order to activate the CMOS inverter stages
  - This stage inverts the signal because it uses an n-channel MOSFET
- Two high-speed inverting CMOS inverter switch stages are needed to decrease the final pulse width even further
- Current Booster takes the output of the push-pull stages and increases the output current to drive the MOSFET gate capacitance
  - Current is increased because these are two push-pull stages in parallel
- Power MOSFET generates the very high voltage output pulse, but requires a lot of gate current to turn on quickly

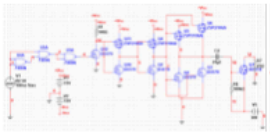


Figure 2: Pulser Circuit Schematic

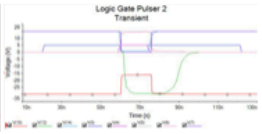


Figure 3: Pulser Circuit Outputs

- Circuit input is dark blue, final output is green
  - Pulse Generator output is purple, Logic Shifter output is light blue, Current Booster Output is pink, Power MOSFET input is red
  - Other lines are inverting push-pull stage outputs
- Note input pulse width compared to output pulse width
- Final output pulse width is wider than pulse width of inverting stages

Future Work:

- Finish testing the pulser output and solder an early prototype
- Design, test, and solder the receiver circuit
- Begin designing and testing adjustable input conditions
- Lay out components using a PCB software
- Design a case and housing for the final product
- Assemble the finished product

Acknowledgements:

- Thanks to Union College, Prof. Buma, SRG Funding, Gene Davison

Appendix D: ECE-499 Slides from 3/2 Presentation Session Week 8 Winter Term

Electrical Engineering

Designing a Low-Cost Ultrasound Pulser

By Andrea Huey

Advisor: Professor Takashi Buma

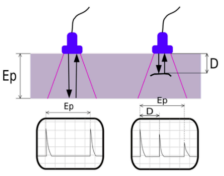
March 2, 2019

Overview of Problem

Ultrasound Imaging

- High-functioning device
  - Allows for precise imaging
  - Very expensive
- Low-cost alternative
  - Loss of extreme precision
  - Costs much less

https://en.wikipedia.org/wiki/Ultrasound



https://en.wikipedia.org/wiki/Ultrasound

UNION COLLEGE

Project Goals

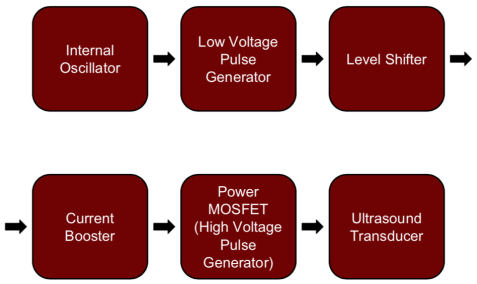
Produce Same Basic Functionality

- Pulse width
  - base goal: <100 ns
  - higher function goal: variable from 20 ns - 100 ns
- Achieve full pulse depth
  - determined by output of high voltage power supply
- Pulse repetition frequency
  - base goal: 1 kHz
  - higher function goal: variable from 1 kHz - 20 kHz
  - external trigger
- Receiver
  - amplification of received signal
  - protection circuitry

UNION COLLEGE

Ultrasound Pulser Overview

Block Diagram of Overall Device

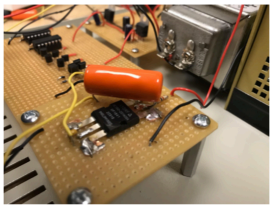


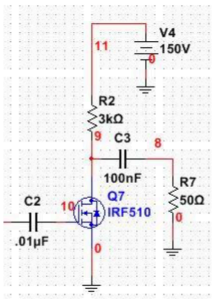
UNION COLLEGE

Power MOSFET

Specifications and Further Details on Final Stage

- High drain-source voltage
  - 200V max
- Fast turn-on time
  - 4 ns
- Drain voltage is final circuit output



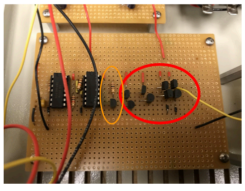


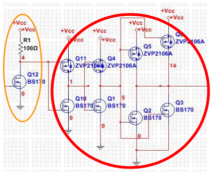
UNION COLLEGE

Current Booster

Two major stages

- Level shifter/Inverter stage
  - raises internal oscillator output magnitude to 15V from 5V
  - stabilises signal and further decreases pulse width
- Current Booster
  - two push-pull stages in parallel double the current output
  - MOSFET needs to get 180 mA of current quickly to turn on



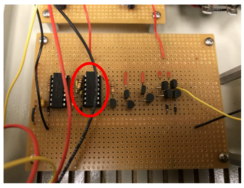


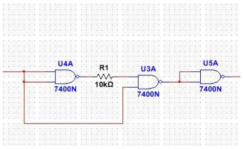
UNION COLLEGE

Low Voltage Pulse Generator

Implemented with digital logic

- Takes advantage of propagation delay in digital logic to trigger a very fast pulse
- Propagation delay was not enough to trigger pulse on its own; required delay resistor in order to achieve desired results



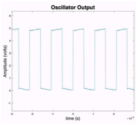


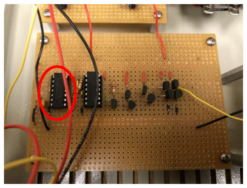
UNION COLLEGE

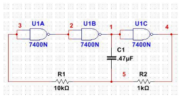
Internal Oscillator

Three Options:

- 555 timer
  - comes as an integrated circuit
  - more difficult to pick correct component values
  - output did not match calculated expectations
- Logic gate oscillator
  - easy to implement using digital logic
  - component values easier to determine
  - output more stable
- Start with high clock
  - divide down





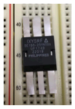


UNION COLLEGE

Major Component Choices

Components Most Necessary to Produce Desired Results

- High voltage power supply
- Power MOSFET
- Internal oscillation method
- Device housing

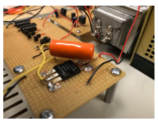


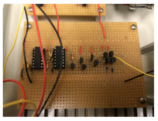
UNION COLLEGE

Power Supplies

3 Separate Voltage Values Required

- 150V
  - high voltage required for deep negative pulse
  - purchased high voltage power source
- 15V
  - required to power MOSFETs from current booster stage
  - used 8.6:1 transformer to step down 120VAC to 14VAC
  - designed rectifier circuit
    - output tied to voltage regulator designed for 15V
- 5V
  - required to power digital logic chips
  - 15V line tied to input of 5V voltage regulator

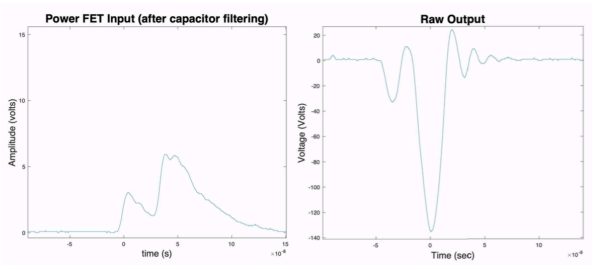




UNION COLLEGE

Preliminary Results for Final Device

Plots Demonstrating Soldered Circuit Behavior

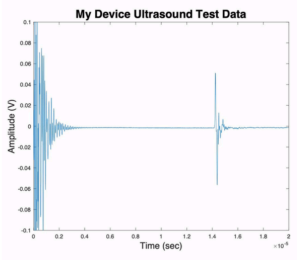


UNION COLLEGE

Test Results

Data on Circuit Output and Use with Transducer

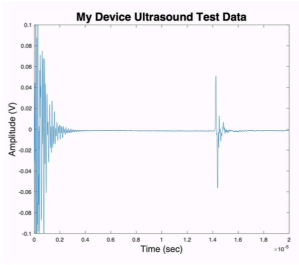
- Connected output of circuit to ultrasound transducer
- Sent a pulse through water to a receiver
- Measured received pulse using digitizer connected to MATLAB

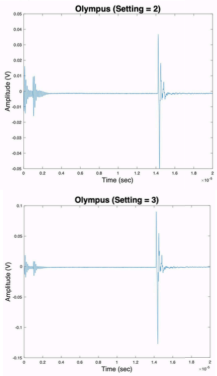


UNION COLLEGE

Comparison to Industry Device

My Device on Left;
Industry Device on Right





UNION COLLEGE

Conclusion

Goal	Achieved?
Pulse width <100ns	☺
Pulse depth reaches -150V	☺
Oscillation frequency 1kHz	☺
Adjustable frequency	☹
Adjustable pulse width	☹
External Trigger	☹
Receiver	☹
Low-cost	☺

UNION COLLEGE

Future Work

Design Input Adjustments and Receiver Circuitry

- Variable pulse width
  - Change delay resistor
- Variable frequency
  - Change timing resistor
- External trigger
  - Include method of bypassing internal oscillator to trigger output off external input
- Design receiver circuitry
  - Return signal will be on the scale of millivolts
    - Must filter out noise while retaining signal data
  - Receive will be routed through same cable as output
    - Requires protection circuitry

UNION COLLEGE

Questions?

Thanks to Professor Buma, Gene Davison, SRG Funding, ECBE Department, and ECE Capstone Students

UNION COLLEGE

Additional Data

Overall Image of Soldered Circuit and Outside of Device

UNION COLLEGE

Additional Data

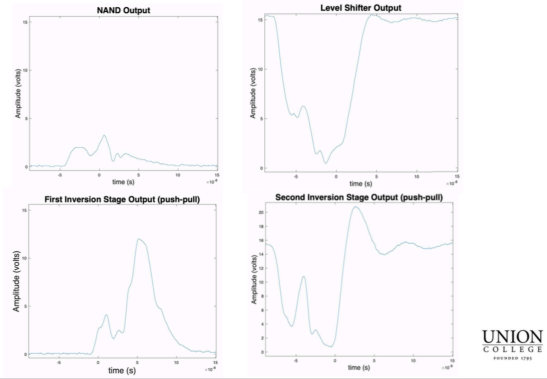
Determination of Resistor/Capacitor Values

- Internal Oscillator
  - 1 kΩ typical R1 value
  - using formula f=1/(2.2*R1*C), determine capacitor value for 1 kHz oscillation to be .47 uF
  - R2 typically 10x R1
- Low Voltage Pulse Generator
  - chose lowest resistor value that still provided full output pulse depth--10 kΩ
- Level Shifter
  - 100 Ω between +15 V and MOSFET gate
- Power MOSFET
  - 100nF capacitor provided best response time
  - 3 kΩ resistor keeps current out of HVPS ~50 mA

UNION COLLEGE

Additional Data

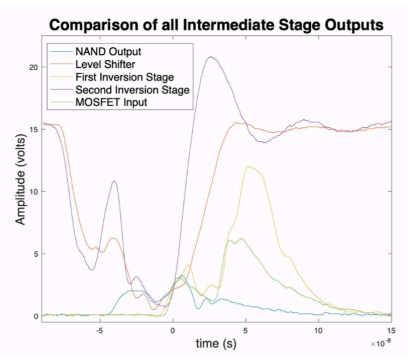
Signal at Various Stages



UNION COLLEGE

Additional Data

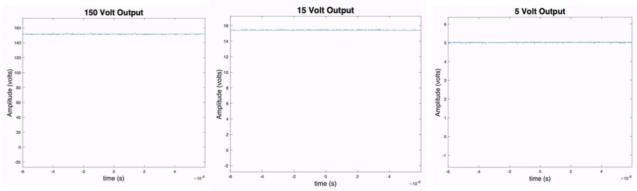
Comparison of Signal at Various Stages



UNION COLLEGE

Additional Data

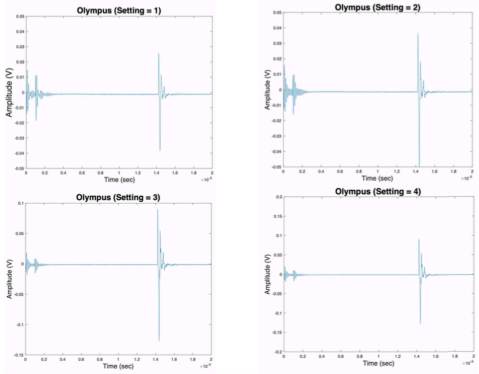
Proof of Voltage Levels



UNION COLLEGE

Additional Data

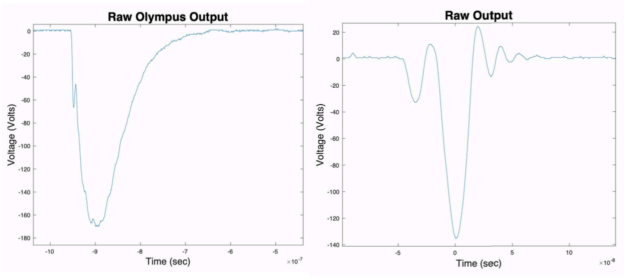
Olympus Energy Levels Compared



UNION COLLEGE

Additional Data

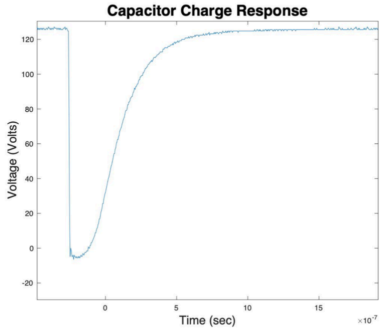
Comparison of Raw Outputs



UNION COLLEGE

Additional Data

Capacitor Charging Response



UNION COLLEGE

Sources

[1] Olympus, "Manually Controlled Pulser-Receivers," 5072PR datasheet, 2009.
[2] J. A. Brown and G. R. Lockwood, *A Low-Cost, High-Performance Pulse Generator for Ultrasound Imaging,* IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control., vol. 49, no. 6, June 2002, pp. 848-851.
[3] J. K. Poulsen, *Low Loss Wideband Protection Circuit for High Frequency Ultrasound,* IEEE Ultrasonics Symposium, 1999, pp. 823-826.
[4] L. Svilainis and V. Dumbrava, *Design of a Low Noise Preamplifier for Ultrasonic Transducer*, Ultragarsas, vol. 55, no. 2, November 2005, pp. 28-32.
[5] Texas Instruments, "420-MHz High-Speed Current-Feedback Amplifier," THS300 datasheet, July 1998 [Revised September 2009].
[6] Texas Instruments, "LFx5xJFETInput Operational Amplifiers," LF356N datasheet, May 2000 [Revised November 2015].
[7] IXYS RF, "DE150-501N04A RF Power MOSFET," 501N04A datasheet, 2009.
[8] Intersil, "5.6A, 100V, 0.540 Ohm, N-Channel Power MOSFET," IRF510 datasheet, November 1999.
[9] Fairchild Semiconductor, "BS170 / MMBF170 N-Channel Enhancement Mode Field Effect Transistor," BS170 datasheet, March 2010.
[10] Supertex, Inc. "N-Channel Enhancement-Mode Vertical DMOS FETs," VN2106 datasheet, 2008.
[11] Supertex, Inc. "P-Channel Enhancement-Mode Vertical DMOS FET," VP2106 datasheet, 2009.
[12] Texas Instruments, "SNx4HC00 Quadruple 2-Input Positive-NAND Gates," SN74HC00N datasheet, December 1982, [Revised July 2016].
[13] IXYS RF, "DE150-201N09A RF Power MOSFET," 201N09A datasheet, 2012.
[14] Acopian, "Gold Box UNREGULATED AC-DC single output & wide adjust output," U400Y20 datasheet.
[15] Hamamatsu, "Compact High Voltage Power Supply C4900 Series," C4900 datasheet, June 2012.
[16] Acopian, "Gold Box LINEAR REGULATED AC-DC single output Series A & B," B150GT10 datasheet.
[17] Hammond Manufacturing, "Class 2 Energy Limiting Small Box Mount," BD2EE datasheet, 2018.
[18] TE Connectivity, "SRB Series," 1SSRBP datasheet, June 2011.
[19] Philmore, "Master Catalog," Miniature Lighted Rocker Switches datasheet, 2012.
[20] Electronics Tutorials, "Stable NAND Gate Waveform Generator," [online]. Available: https://www.electronics-tutorials.ws/waveforms/generators.html. [Accessed: 2-14-2019]

UNION COLLEGE
FOUNDED 1795

Appendix E: ECE-499 Poster from 3/11 Poster/Demo Session Week 10 Winter Term

Senior Project – Electrical Engineering and English Double Major – 2019

Designing a Low-Cost Ultrasound Pulser

Andrea Huey
Advisor – Prof. Takashi Buma

Introduction:

- Ultrasound imaging is an incredibly powerful technology that grants the ability to see inside a patient or subject without cutting them open
- Ultrasound pulse transmitted by applying high voltage pulse to an ultrasound transducer
- Same transducer detects echoes, which are amplified to obtain data and reconstruct an image
- Commercial pulser/receivers can cost several thousand dollars
- Professor Buma needs a low-cost alternative so he can conduct experiments with multiple ultrasound devices

Design Requirements:

- Pulser shall produce a -150 V spike
- Duration of voltage spike should be <100 ns
  - Adjustable pulse width from 20 ns - 100 ns desired
- Basic repetition rate of 1 kHz
  - Adjustable repetition rate from 1kHz-20kHz desired
- 2 different trigger options desired
  - Internal trigger that keeps time and self-triggers
  - External trigger that operates on 0-5V logic scale
- Most obvious requirement is cost since this is a a low-cost alternative

Results:

- For testing, connected my pulser to an ultrasound transducer and used it to send an ultrasound pulse to a receiver
- Was able to successfully produce ultrasound pulse, receiver connected to digitizer made received waveform easier to save in MATLAB

Figure 4: Device Ultrasound Test

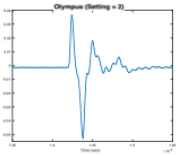


Figure 5: Olympus Setting 2

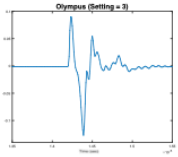


Figure 6: Olympus Setting 3

- My device's output magnitude falls somewhere between energy settings 2 and 3 on the Olympus 5072PR device
- Beginning of signal (not pictured) has more noise; this could likely be eliminated through implementation of filtering

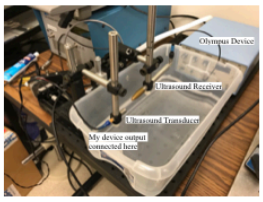


Figure 7: Test Setup

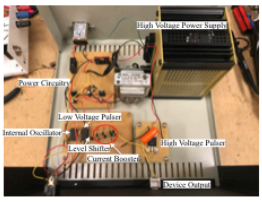


Figure 8: Final Device Configuration

Design:

- The pulser consists of five primary stages, the output of which is tied to an ultrasound transducer

Figure 1: Block Diagram of Pulser Circuit

- Internal Oscillator is a simple NAND gate oscillator which provides the desired 1 kHz repetition rate
- Low Voltage Pulse Generator provides the initial pulse that is eventually carried through the circuit to the final output
- Level Shifter raises voltage magnitude from 5 V logic output to 15 V MOSFET and further stabilize the signal
- Current Booster doubles the current carried through the circuit, which provides the gate of the power MOSFET to current (180 mA) to turn on
- High Voltage Pulse Generator provides final circuit output, which is that fast negative voltage spike that drives the ultrasound transducer
  - Pulse generated with a high power MOSFET
    - (max drain-source voltage = 200V; turn-on time = 4 ns)
  - High voltage power source (HVPS) cannot provide necessary current to drive load, must find alternate source that can provide 3 A
    - Solution is charging a high voltage capacitor with the HVPS, meaning the capacitor is delivering the current, not the HVPS

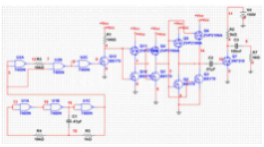


Figure 2: Pulser Circuit Schematic

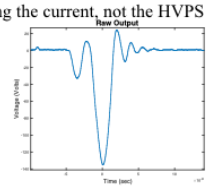


Figure 3: Pulser Circuit Output

Conclusions and Future Work:

- Achieved base pulse width of <100 ns, base repetition rate of 1 kHz, and full pulse depth of 150 V, as well as low-cost requirement
- Adjustable pulse width — vary value of delay resistor
- Adjustable pulse repetition rate — vary value of timing resistor
- External trigger — way of bypassing internal oscillator or way of turning it on and off due to an external input
- Design receiver circuitry — must amplify millivolt pulse and protect it from high voltage output (shared BNC connector)

Acknowledgements:

- Thanks to Union College, Prof. Buma, SRG Funding, Gene Davison