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The design, development and construction of a low cost multi-purpose computer/interface system for on-line experimentation: applications to time averaging of NMR spectra and other chemical instrumentation problems

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THE DESIGN, DEVELOPMENT AND CONSTRUCTION OF A LOW COST MULTI-PURPOSE COMPUTER/INTERFACE SYSTEM FOR ON-LINE EXPERIMENTATION: APPLICATIONS TO TIME AVERAGING OF NMR SPECTRA AND OTHER CHEMICAL INSTRUMENTATION PROBLEMS

by

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ABSTRACT

CARR, STEVEN ALFRED The Design, Development and Construction of a Low Cost Multi-Purpose Computer/ Interface System for On-Line Experimentation: Applications to Time Averaging of NMR Spectra and Other Chemical Instrumentation Problems. Department of Chemistry, June 1976.

The project goal was the development of a low cost multi-purpose microprocessor interfacing system that would be adaptable to a number of commonly encountered chemical instruments (such as NMR, GC, IR, and UV-VIS.) for the purpose of control, data acquisition and processing.

The Altair Microprocessor with 4K random access memory was constructed from kit form; it functions as the computer portion of the system. The digital to analog and analog to digital signal conversion elements as well as timing, control and other necessary logic functions are incorporated in the electronic interface portion of the the system. The computer, interface, principles of time averaging, and the philosophy of interfacing in general, are the subjects of this report.

The Perkin Elmer R-24A NMR spectrometer is presently attached to the computer/interface system so that signal time averaging on low concentration samples may be accomplished. A by-product of this particular system is a library of spectra stored on binary coded paper tape which can be used to generate spectra without having to make up samples.

Future applications of the system are also considered in this thesis.

To Christa

I learned this at least by my experiment: that if one advances confidently in the direction of his dreams, and endeavors to live that life which he has imagined he will meet with success unexpected in common hours.

Henry David Thoreau

I would like to gratefully acknowledge the invaluable assistance of Dr. Leslie Hull and Dr. Thomas Werner of the Chemistry Department at Union College, and Dr. George Williams of the Electrical Engineering Department.

Special thanks go to Arthur Fritzson of the Computer Science Department who made the interface 'come alive' with his computer programs, to my father who patiently taught me all the electronics I know, and to my mother, who didn't quite understand what I was doing, but loved me just the same.

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STEVEN ALFRED CARR

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CHAPTER I

SIGNAL TIME AVERAGING, INTERFACING AND DIGITAL ELECTRONICS

A. INTRODUCTION

Since the development of the principle of Nuclear Magnetic Resonance in 1946 by Block at Stanford and Purcell at Harvard[1] methods of sensitivity enhancement have been searched for in its use as an illuminator of structural detail. As powerful an analytical tool as the NMR is it still requires fairly high sample concentrations (usually 2 to 15% v/v) compared to other spectral absorbance techniques. Numerous approaches have been found to circumvent

this problem when sample sizes have excluded the NMR's normal use. Among these are: 1) increased magnetization of the sample through higher excitation field strength and/or lower temperatures, 2) Overhauser experiments, 3) use of intermediate passage conditions[2], 4) optimization of the sample receiver circuitry and the probe assembly and through use of bandpass and band reject filters, 5) use of Fourier transform techniques and 6) the use of signal time averaging[3]. The last two provide the greatest sensitivity enhancement but due to the prohibitively high cost, such instrumentation has not been available to small undergraduate institutions such as Union College. However with the advent of Large Scale Integrated circuits (LSI) in the 1960's and Metal Oxide Semiconductors (MOS) around 1970[4], the price and size of complex digital electronic circuit elements have dropped sufficiently to allow construction of a signal time averager (computer of average transients as it is sometimes called, CAT) from digital logic circuit blocks and the "computer on a chip" type of digital microprocessor at very reasonable cost. With such a device, useable spectra can be obtained on as little as 150 μg of sample[5]. This report is about the building of just such a system.

The principle behind time averaging is quite simple; normally one scan is used to produce an NMR absorption spectrum. If sample concentration is too low however an

increase in amplifier gain will result in both an increase in signal amplitude and noise amplitude. Of course if the signal is "buried" in the base-line noise then amplification will do little to resolve a spectrum. The noise present in the spectrometer comes from many sources but all forms present fall into two categories: inherent noise and induced noise. Inherent noise is generated primarily by the source resistance of the sample detector, preamplifier and amplifier circuits. Induced noise is a product of the environment external to the instrument; this is noise which is picked up through magnetic, galvanic or electrostatic coupling to the power supplier, detectors, amplifiers and logic circuits. Both types of noise fall into two further subdivisions: random and coherent. Random noise is produced in components such as resistors, semiconductors junctions and transformer cores[6]. Coherent or "non-white" noise is produced via thermal drift, microphonic noise, modulation/demodulation processes or it can be coupled in from the outside world in the form of line spikes etc. If all of the noise generated in the NMR is random, then the signal to noise ratio of the output will increase proportionally to the square root of the number of scans[7].

In order to utilize this method the output of the spectrometer must be coupled via a digital processing network to a computer memory. Successive scans of equivalent

length are sampled by an analog to digital convertor and are added to previous samples already in computer memory. The signal being a coherent function of time will add, whereas the noise, which is a random function of time, will average out to zero. The "$\sqrt{n}$ law" is not always strictly obeyed due to autocorrelation effects, fast scan rates or if the power spectrum is not a reasonably smooth function of the frequency[8].

B. NMR SPECTROSCOPY AND THE NMR SPECTROMETER

In order to understand how a time averaging system functions, it is first necessary to examine the information that is to be averaged and how it is produced; this entails an understanding of Nuclear Magnetic Resonance and the operation of an NMR spectrometer.

When the nuclei of certain elements are exposed to a strong external magnetic field splitting of the nuclei into 2 or more well defined energy levels occurs. Transitions between these energy levels can be caused by absorption of electromagnetic radiation of a particular frequency. To account for these characteristics we must look at some of the intrinsic properties of particles. All nuclei have a

net spin momentum which is a quantized amount corresponding to the particular nuclei. These quantized angular momenta are given by:

$$\frac{h}{2\pi}\,(I\,(I+1)) \quad \text{Eqn. 1-1}$$

where "I" is the nuclear spin quantum number and h is Planck's constant. I = 0 denotes no spin; I may take on values of 1/2, 1, 3/2 etc., depending on the resultant of the proton + neutron spins. If the number of neutrons plus protons is even I = 0 or an integral; if it is odd, I is a half integral. If the number of both neutrons and protons is even then I = 0. Such is the case with ^{12}C and ^{16}O.

Since nuclei are charged and spinning charges create magnetic fields we create nuclear magnetic dipoles whose intrinsic magnitude is assigned as "μ", the nuclear magnetic moment. The value of μ is different for each particle, and the direction of μ is colinear with the angular momentum vector.

$$\gamma = \frac{2\pi\mu}{Ih} \qquad \mu = \frac{\gamma h}{2\pi}\ I \quad \text{Eqn. 1-2}$$

where γ = the magnetogyric ratio which is a constant for a given nucleus.

The above relation expresses the proportionality existing b/w the magnetic moment and the angular momentum of the rotating particle.

Within an externally applied uniform magnetic field, "H_o", the number of orientations that a nucleus may assume is given by (2I + 1). The spin number for protons is + 1/2 and - 1/2. These are therefore 2 positions that a proton may assume in the H_o field: with it (induced field in direction of applied field) or against it. The parallel configuration is a low energy stable state, whereas the antiparallel state is a high energy, unstable one.

Excitation occurs when a photon of an energy equivalent to energy gap ΔE is absorbed by the nuclei. Since

$$E = h\nu = \frac{\mu\beta H_o}{I} \qquad \text{Eqn. 1-3}$$

the frequency of the transition is given by:

$$\nu = \frac{\mu\beta H_o}{hI} \qquad \text{Eqn. 1-4}$$

, where β is a constant called the nuclei magneton[9].

The P.E. R-24 A NMR spectrometer utilizes a 60 MHz excitation frequency and a main field strength (H_o) of 14,100 Gauss shunted to 14,092. If

$\Delta E = h\nu$ h = Planck's constant Eqn. 1-5

ν = frequency

than $\Delta E = (6.62 \times 10^{-27}$ erg/sec$)(60 \times 10^{6}$ Hz)

$= 4 \times 10^{-19}$ erg = 0.05 cal/mole.

At room temperature we have approximately 600 cal/mole, therefore before the field is applied we have enough energy to populate the upper level. The fact that the energy of excitation is very small is both the reason for the NMR's usefulness as an analytical tool and its inherent insensitivity. The small energy of excitation allows the probing of a molecules structure without disrupting the chemical bonds; however the population difference as given by the following equation:

$$\frac{n \text{ upper}}{n \text{ lower}} = e^{-\Delta E/RT} \qquad \text{Eqn. 1-6}$$

shows that for every 10×10^{6} nuclei only 20 more are in the lower E level than in the upper; obviously the sensitivity of the receiver must be great and the sample size must be large. (The lower level population is maintained through relaxation processes[10] which are beyond the scope of this thesis.)

Wrapped around one of the poles of the magnet are the sweep, shift and feedback coils (see Figure 1-1a). It is

Figure 1-1a Block diagram of the model R-24A NMR spectrometer.

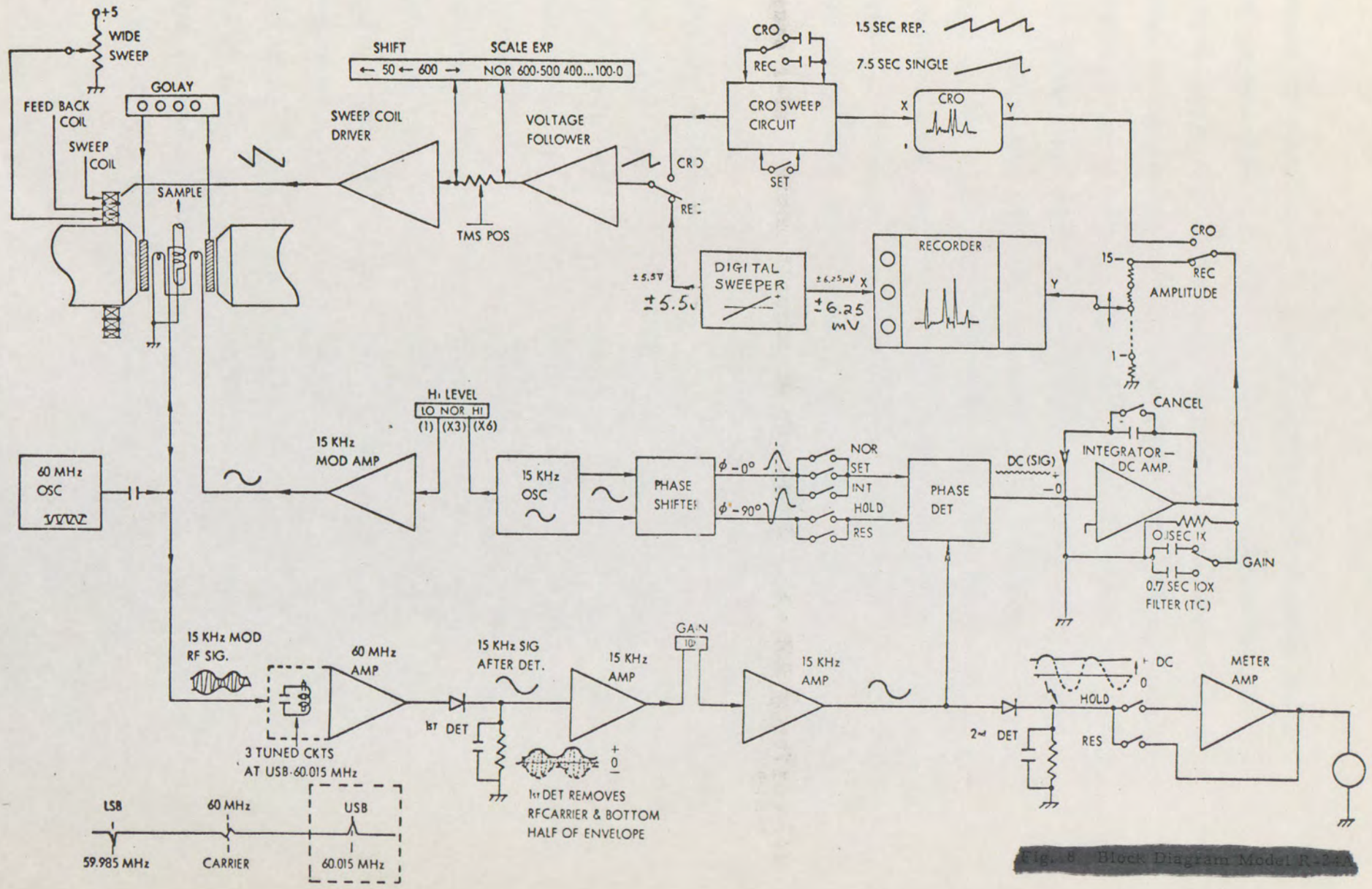


Fig. 8 Block Diagram Model R-24A

necessary to sweep over a range because all protons do not absorb at the same ν; this is due to the precessing of electrons about the nuclei which induces a magnetic field opposite in direction to the opposed field. This "shields" the nuclei from the full strength of the H_o field to varying degrees depending upon the electron density at the given nuclei. In theory either the excitation frequency or the strength of the main magnetic field may be varied to scan the spectrum (see equation 1-3). Most NMR's however sweep the magnetic field over a small range (0-10 ppm corresponding to 1000 Hz in 60 MHz) by passing a sawtooth current through the sweep coil; in the R24A this pulse originates either in the sweep generator or the digital sweeper circuit, depending on the mode of operation[11].

Homogeneity of the main magnetic field is obtained through precise adjustment of a series of nine golay coils situated about the sample area; adjustment of these coils constitutes the tuning of the NMR which is necessary to restore parallelism of the flux field which is usually destroyed by the presence of the sample tube and probe assembly. Spinning of the sample removes any residual field inhomogeneities on the horizontal axis. Linearity of the field is also highly temperature dependent, thus the entire magnet and probe assembly is thermostatted.

The sample probe contains the 60 MHz excitation coil and 15 KHz coils; these two types of coils are mutually

perpendicular. Crystal controlled oscillators supply the correct pulse widths. The simultaneous application of differing frequencies to a circuit containing a non-linear impedance (represented here by the reactive inductance of the coils) will produce an output which will contain the main frequency, in this case 60 MHz, as well as two new frequencies - one equal to the sum and one the difference of the 15 KHz and 60 MHz frequencies. This produces a lower side band at 59.985 MHz and an upper side band at 60.015 MHz. When a difference signal is produced through sample absorption, amplitude changes in the side bands result. The probe assembly output is coupled to a 60 MHz RF amplifier tuned specifically to the upper side band of the amplitude modulated signal.

The 60 MHz excitation frequency is removed by the first detector; this signal is then amplified and fed to a phase detector where the in phase component is converted to a DC signal, amplified, and then fed to either the cathode ray oscilloscope (CRO) or the x-y recorder.

The above discussion was focused on the signal path in the NMR; however, for time averaging purposes we must also know precisely how the field is swept and how the position in the field is synchronized to the "position" of the sweep coil; i.e., how do the NMR and recorder maintain an exact field to frequency relationship? The P.E. R-24A accomp-

lishes this through the application of digital electronics in the sweeper circuit. The digital sweeper is comprised of an oscillator, up/down digital counters, digital gating logic and a digital to analog converter. Even for the chemist acquainted with electronics, the digitization of information may at first glance seem mysterious; therefore a detailed examination of digital circuit elements is contained in Chapter I, Section D of this report.

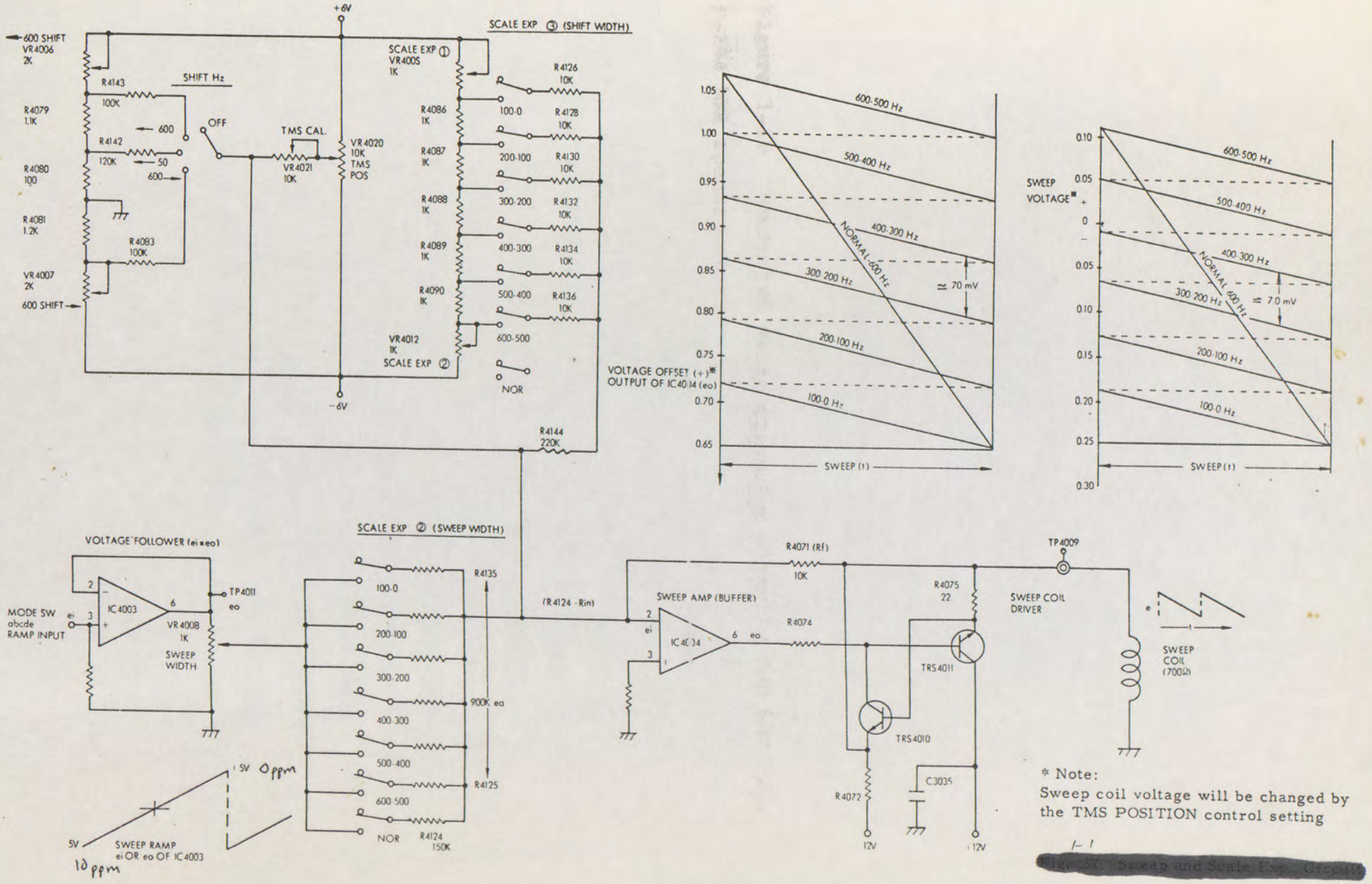
The output of the digital sweeper is a linear ramp voltage which varies from 10.0 v to -10.0 v. An operational amplifier[1] scales this voltage down and provides two outputs: $\pm$5.5 v for the field sweep, and $\pm$6.3 mV for the recorder X axis sweep.

The field sweep portion of the output is fed into another operational amplifier wired in the voltage follower configuration so that it serves as a unity gain amplifier (see Figure 1-1b). Scale expansion is accomplished by utilizing a bank of precision resistors, individually selectable through pushbutton switches on the front panel, as the R_{INPUT} elements of the sweep amp buffer IC 4004. The output voltage range of the buffer is determined by the following formula:

---

1 For an excellant discussion of operational amplifiers see "ANALOG TO DIGITAL CONVERSION HANDBOOK", D. H. Sheingold ed., ANALOG DEVICES INC., NORWOOD MASS., Part III Ch. 1.

Figure 1-1b Sweep and scale expansion circuits for the P.E. R-24A NMR spectrometer.



* Note:
Sweep coil voltage will be changed by the TMS POSITION control setting

/- 1

[redacted]

[redacted]

14

$$E_o = \frac{R_{FEEDBACK} = R4071 = 10K\Omega}{R_{INPUT}} \times E_{IN} \qquad \text{Eqn. 1-7}$$

where E_o is the voltage at pin 6 IC 4004 and E_{IN} is the output of IC 4003.

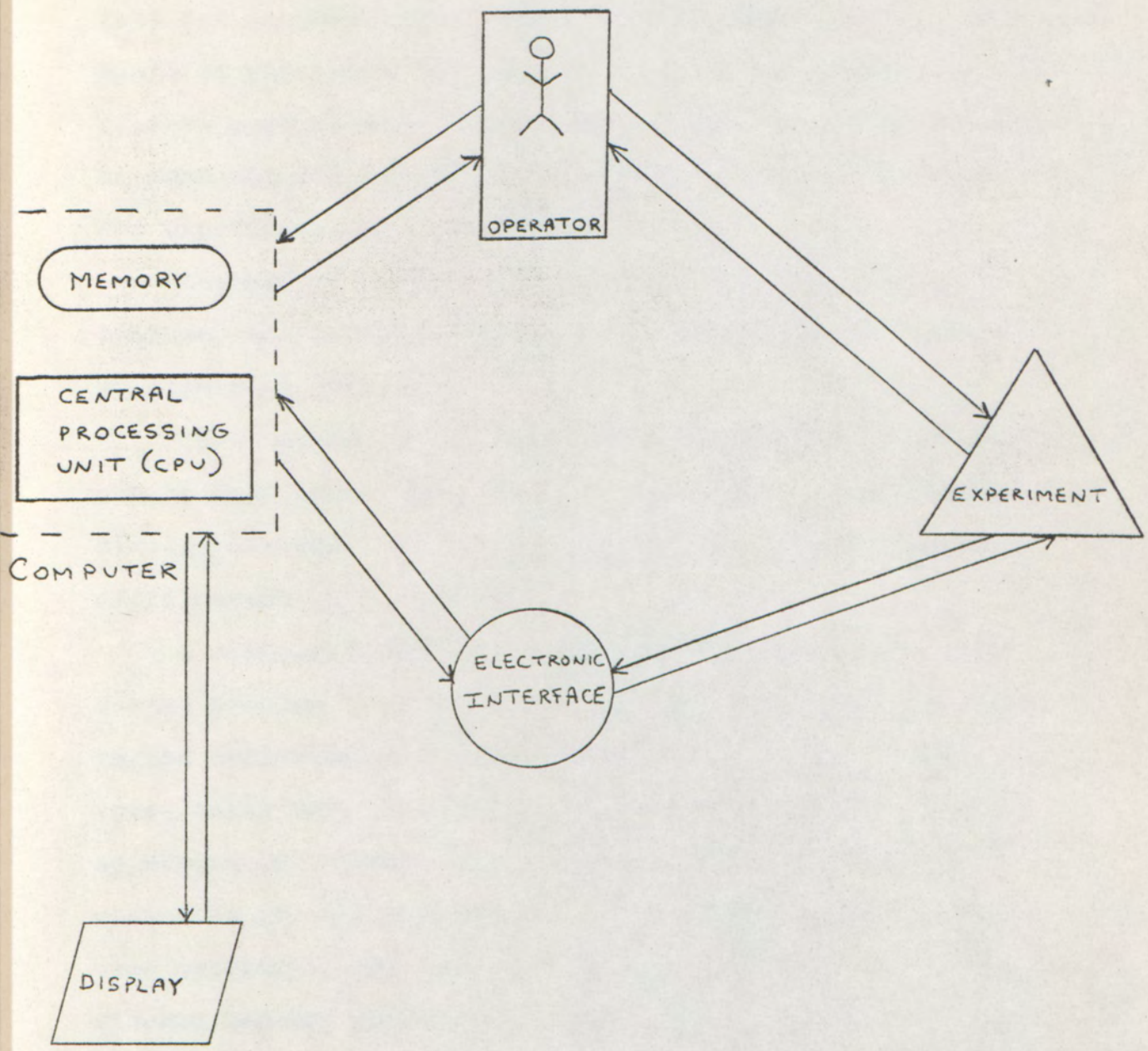
The sweep amp IC drives transistor 4011 which in turn applies voltage to the sweep coil itself.

C. DEFINING THE INTERFACING PROBLEMS

The project involves the interfacing of an Altair 8800 4K random access microprocessor, representative of a new generation of small digital computers, with Perkin Elmer's model R-24A NMR for the purpose of signal time averaging.

A generalized system configuration is illustrated in Figure 1-2. The important point to note is that there exists a direct communications link between the computer and the experiment. Most scientists are used to off-line computer systems in which the operator interacts with the experiment, and then in turn feeds data in specified form along with a program written in a language such as FORTRAN, to instruct the computer on how the data is to be handled. Turn around times can often be quite long.

Figure 1-2 Generalized on-line computer operation.


OPERATOR
MEMORY
CENTRAL PROCESSING UNIT (CPU)
COMPUTER
EXPERIMENT
ELECTRONIC INTERFACE
DISPLAY

In the present case the computer and the experiment are directly connected via an electronic interface. The interface can contain many different elements but usually consists of electronic circuits for timing and synchronization of data acquisition, control logic, and conversion modules to make the digital computer understand the analog world of the experiment, and vica versa[12].

Instead of paper punch cards for the inputting of a program, the program must either be in memory or readily available to memory.

Upon completion of the experiment computational results can be made immediately available to a wide variety of display devices such as a Teletype (TTY), chart recorder, oscilloscope or line printer.

A microprocessor was chosen for the particular interfacing problem in this project because it is ideally suited to the dedicated on-line application that signal time averaging calls for. Its limited memory (4096 8 bit words) is no hindrance to real-time operation in which data is processed as it is being acquired. The computing system has been matched to the task[13]; a larger computer was not considered because there would have been an excess of computing power and memory for single instrument monitoring. In addition processing speed was not of primary importance (microprocessors are much slower than large computers); real

time operation can be employed as long as the data sampling rate does not exceed the time involved for the computer to perform the specified manipulation. Because the larger computer system was not needed cost could be kept way down; the Altair 8800 in kit form with 4 K memory and I/O boards sells for approximately 1000 $.

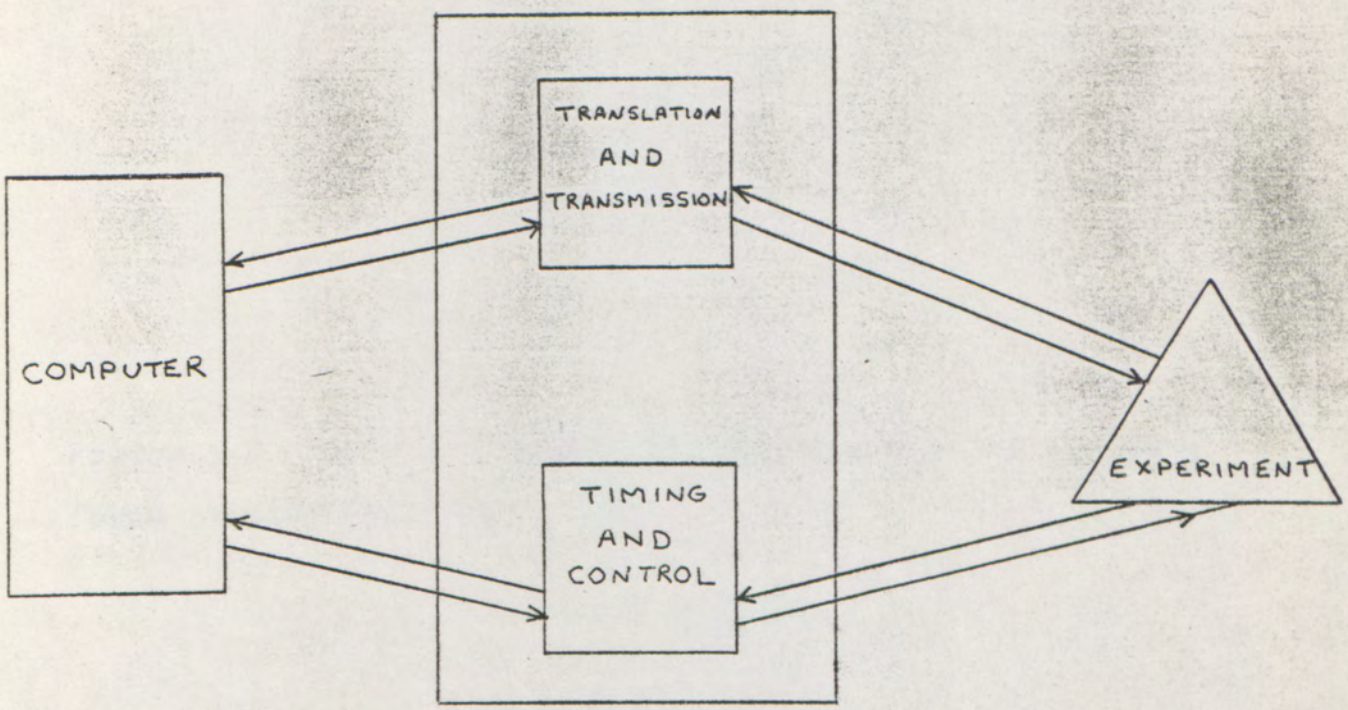
The interface itself may be schematically represented as has been done in Figure 1-3[14]. The translation and transmission elements (further broken down in Figure 1-4) allow understandable communication between the experiment and the computer; timing and control logic allows for synchronization of these two elements (see Figure 1-5).

Many of the circuit elements illustrated in the figures will be discussed along with methods of application in Chapter I Section D and Chapter II of this report.

The signal output of the NMR is an alternating waveform. Normally this output is connected to a chart recorder and an NMR absorption spectrum is obtained. The computer requires digital input, therefore an analog to digital converter (ADC or A/D) device is needed. The ADC has specific voltage input requirements; therefore the output of the NMR must be processed in such a way as to meet these needs (see Figure 1-6).

The R24A P.E. NMR does not have multiscan capabilities built into the instrument. Thus the second interfacing problem was designing a method through which repetitive

Figure 1-3 Expanded view of the electronic interface and its system interconnections.



ELECTRONIC INTERFACE

Figure 1-4 Types of translation and transmission elements found in electronic interfaces.

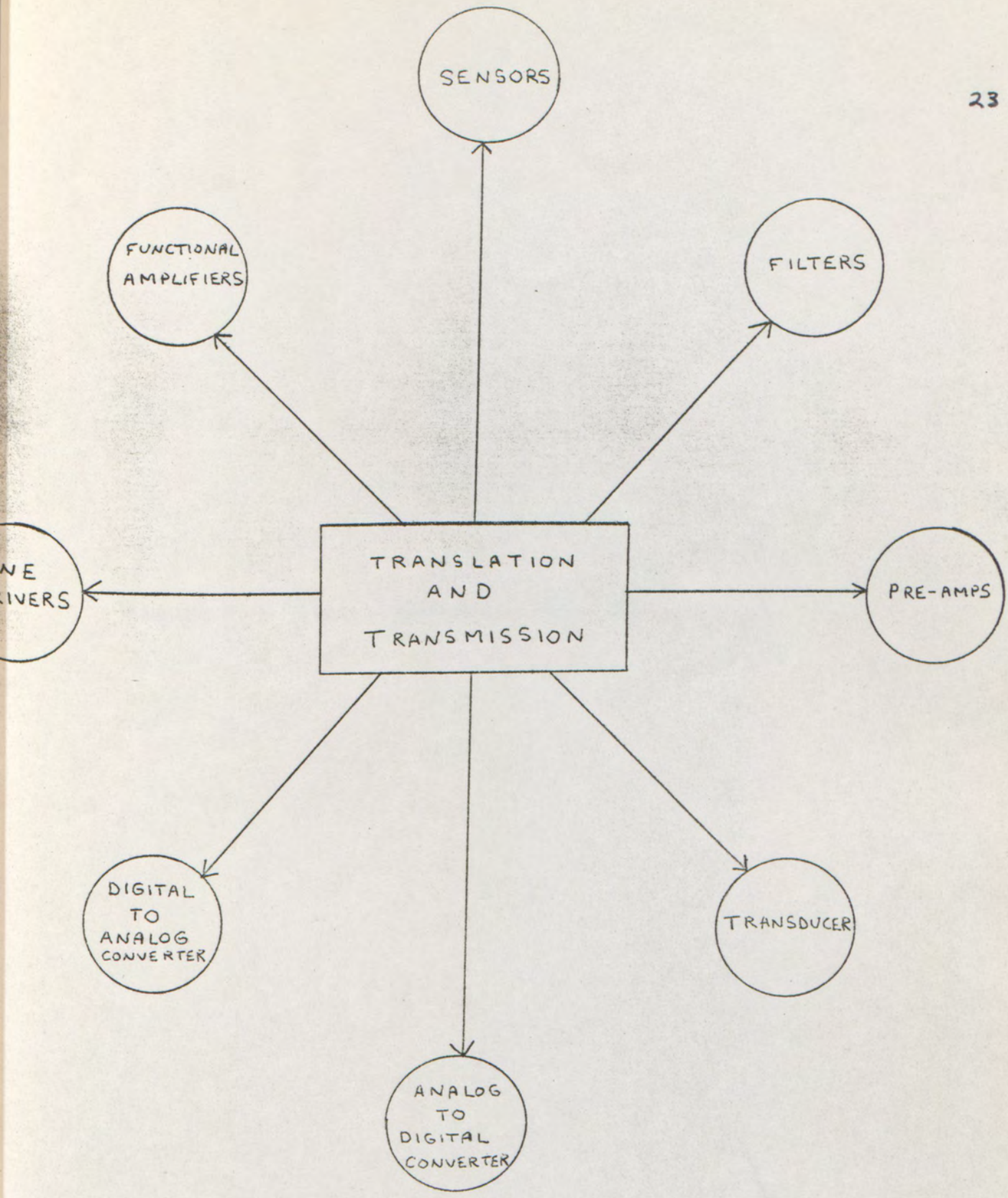

SENSORS
FUNCTIONAL AMPLIFIERS
FILTERS
NE
IVERS
TRANSLATION AND TRANSMISSION
PRE-AMPS
DIGITAL TO ANALOG CONVERTER
TRANSDUCER
ANALOG TO DIGITAL CONVERTER

Figure 1-5 Timing and logic elements.

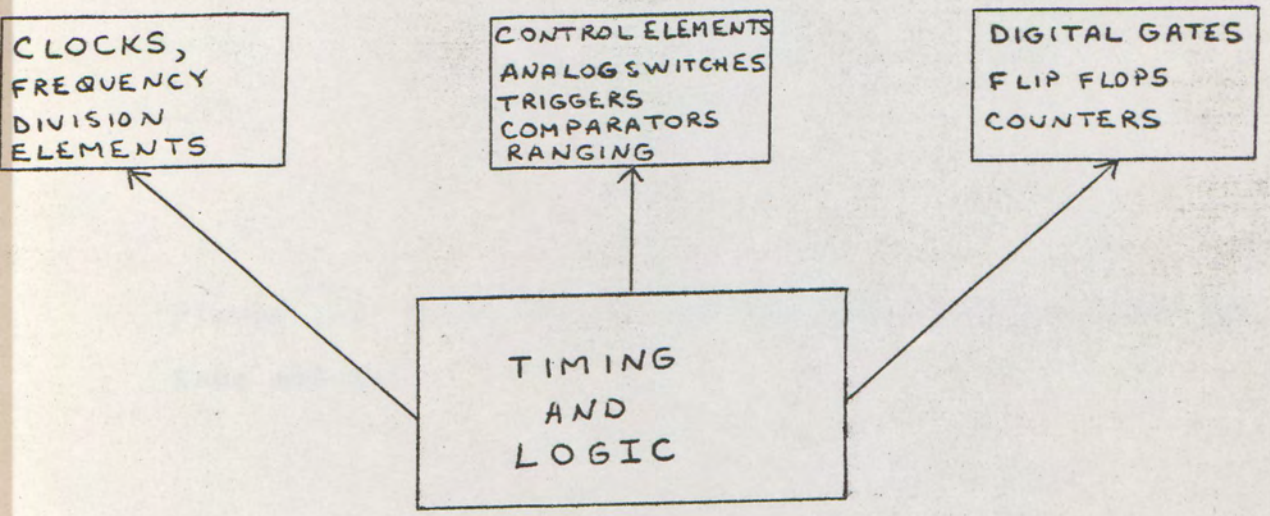
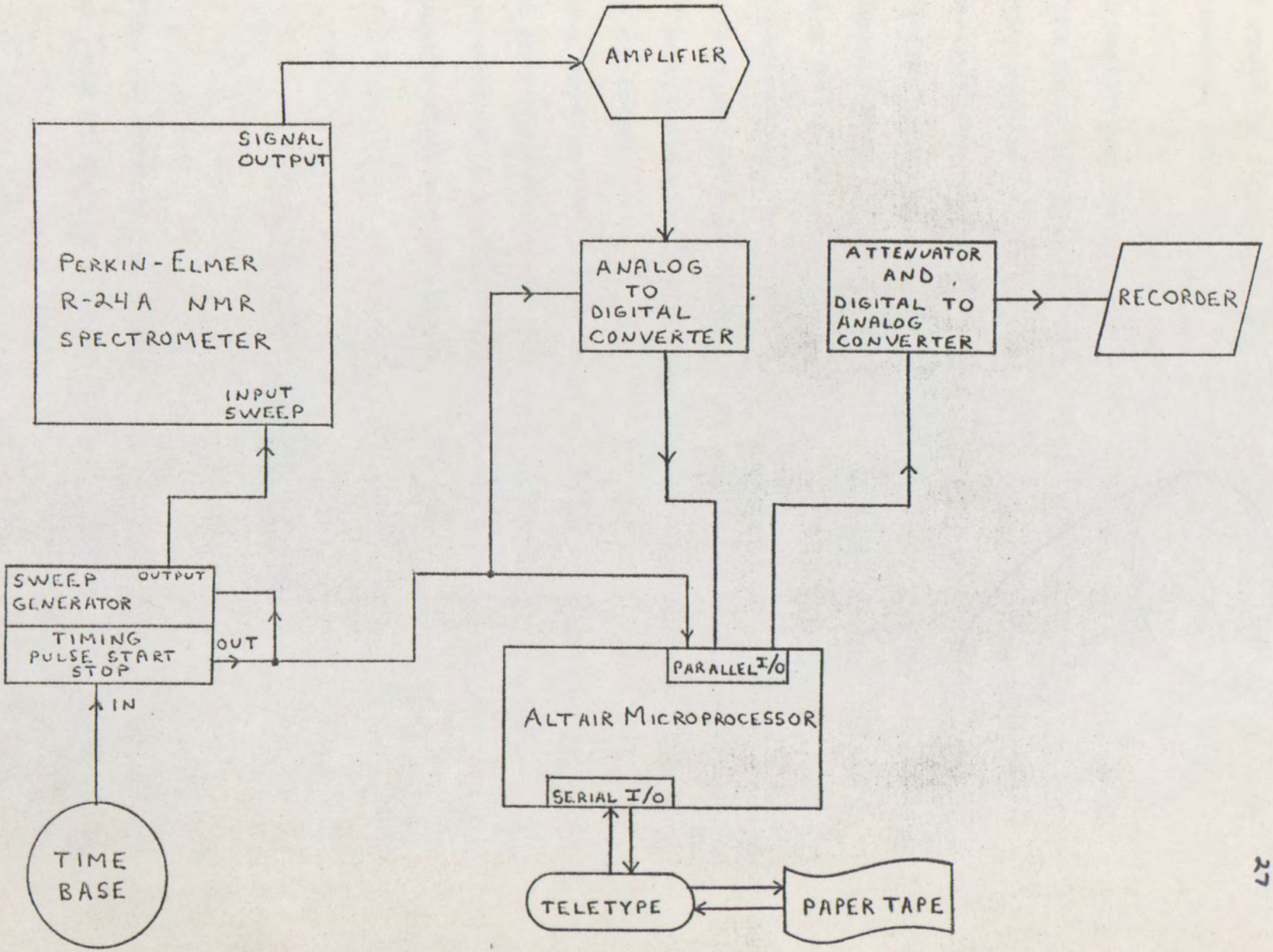

CLOCKS,
FREQUENCY
DIVISION
ELEMENTS
CONTROL ELEMENTS
ANALOG SWITCHES
TRIGGERS
COMPARATORS
RANGING
DIGITAL GATES
FLIP FLOPS
COUNTERS
TIMING
AND
LOGIC

Figure 1-6 Block diagram of the NMR, microprocessor and interface modules.


AMPLIFIER
SIGNAL OUTPUT
PERKIN-ELMER R-24A NMR SPECTROMETER
INPUT SWEEP
ANALOG TO DIGITAL CONVERTER
ATTENUATOR AND DIGITAL TO ANALOG CONVERTER
RECORDER
SWEEP GENERATOR
OUTPUT
TIMING PULSE START STOP
OUT
IN
PARALLEL I/O
ALTAIR MICROPROCESSOR
SERIAL I/O
TIME BASE
TELETYPE
PAPER TAPE

scans could be generated and precise synchronization of the experimental output and the data acquisition process maintained.

Finally the data input to the computer must be averaged with the data already in memory; this of course involves a computer program. The average of the scans can be sent to various peripheral equipment such as an oscilloscope, TTY or a recorder. Once again the requirements for input to the peripherals must be satisfied, thus de-digitization (or in the case of the Teletype parallel to serial conversion) need to be performed. The computer itself may be externally controlled and monitored by a TTY; this is a more efficient way of conversing with the computer than through its console switch register.

The generalized description above is graphically represented in Figure 1-6. The detailed operation and construction of each of the circuit elements will be the topic of much of the rest of the report.

D. A DIGITAL ELECTRONIC PRIMER

This section of the report is an attempt to organize a general body of knowledge that may be appled to the study of

most commonly encountered digital circuit elements. There are five currently popular integrated circuit logic types which differ in the circuit elements used to perform the logic, and the voltage levels necessary to cause the logical transition. These are tabulated below[15]:

Table 1-1 Common IC Logic Types

Abbreviation	Logic Type	Logic Performed By	Logic Voltage Levels
RTL	Resistor-Transitor	Driver Transistors	0, +3.6 v
DTL	Diode Transistor	Input Diodes	0, +5 v
T^2L or TTL	Transistor-Transistor	Input Transistor	0, +5 v
ECL	Emitter Coupled	Input Transistors	-1.55,-0.75 v
HTL	High Threshold	Input Diodes	0, 8-30 v

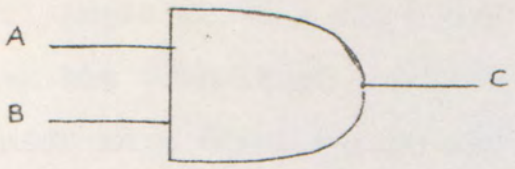
These circuit elements are the foundation upon which most digital instrumentation including computers and interfacing circuits are built. All of the above mentioned types perform the same basic logic functions: AND, OR, INVERT, NAND, NOR. These functions (which will be further explained) are represented by voltage levels. Table 1-2 includes the standard symbolic representation for the microelectronic integrated circuit form of an AND gate. A gate is an electronic device utilized for a particular basic logic func-

tion. In 1854 George Boole a British mathematician developed a system of symbolic logic known as Boolean algebra. The premise upon which his system rested was that if logical reason could be represented by specific symbols then thought processes could be written as algebraic equations. Logic circuits such as the AND gate in Figure 2-2 operate according to Boole's system: either a statement is true or false. On or off, + 5 volts or 0.0 volts (in TTL) are the electronic analog of this concept. A mathematical chart representing the possible logical permutations for a particular gate or combination of gates is known as a truth table. In such a table ON (TRUE) or +5 volts is represented as a "1", whereas OFF (FALSE) or 0 volts is indicated by a "0". Table 1-2 illustrates the five basic logic types along with their respective truth tables.

The reader may verify that the NAND and NOR gates are respectively, AND and OR gates followed by an inverter.

Almost all logic circuits are comprised of the above five elements in some combination. More complex circuit elements that will be discussed later such as counters and flip-flops are built from the gates shown. At this juncture a detailed analysis of one type of integrated circuit logic would be appropriate. TTL logic has been chosen because of its common usage and because TTL logic has been employed in the design of the interfacing circuitry for the NMR.

Table 1-2 Basic electronic gates and truth tables.

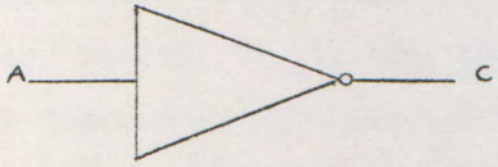


AND GATE

INPUT A	INPUT B	OUTPUT C
1	1	1
0	1	0
1	0	0
0	0	0

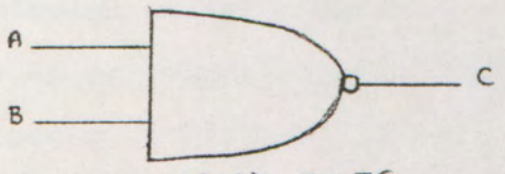
OR GATE

INPUT A	INPUT B	OUTPUT C
1	1	1
1	0	1
0	1	1
0	0	0



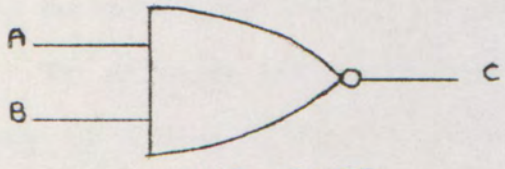
INVERTER GATE

INPUT A	OUTPUT B
1	0
0	1



NAND GATE

INPUT A	INPUT B	OUTPUT C
1	1	0
1	0	1
0	1	1
0	0	1



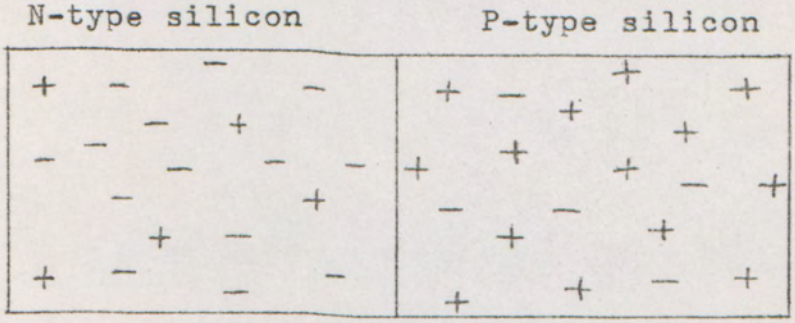
NOR GATE

INPUT A	INPUT B	OUTPUT C
1	1	0
0	1	0
0	0	1

TTL logic devices use conventional bipolar transistors in which the transistor acts as a saturated switch. A transistor is a three region device composed of "N" type silicon or germanium with specific elemental impurities such as phosphorus or antimony which serve as electron doners, and P type silicon or germanium with electron deficient impurities such as boron, gallium or indium which create (+) holes in the crystal lattice[16]. When an N region and a P region are physically connected as shown in Figure 1-7 excess electrons in the N area will flow into the P region and holes in the P area will flow into the N crystal. Buildup of net charge eventually stops the interchange of carriers. To utilize the PN junction as an amplifier an external forward bias is applied which forces charge carriers across the junction via the applied EMF, thereby creating the common silicon diode (see Figure 1-8)[17]. Amplification is achieved because the current flowing in the circuit is exponentially related to the applied voltage, as is indicated in Figure 1-9.

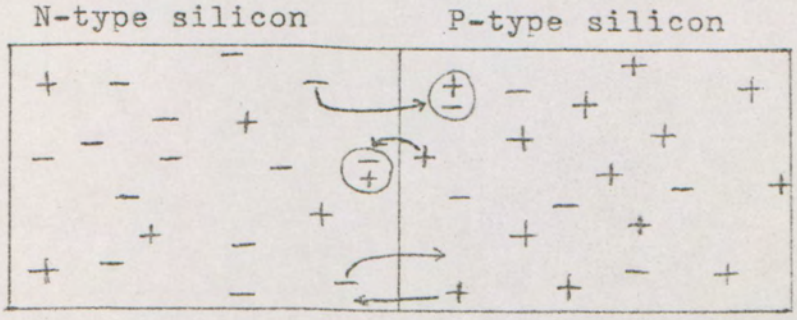
When three regions are put together such that one region is sandwiched between two of the conjugate type a junction transistor is created. Thus an NPN transistor is composed of a narrow P type silicon between two wider N type strips. To utilize this transistor as an amplifier it is necessary to forward bias the emitter and base sections (see Figure 1-10) and reverse bias the collector to base.

Figure 1-7 The formation of the P-N junction; as shown, some recombination of charge carriers occurs, but the electrostatic potential created by those charges which do not combine prevents further movement of charge across the barrier.



PRIOR TO JUNCTION FORMATION

- electron
+ hole
⊕ recombination
⇄ arrows indicate direction of charge migration



JUNCTION FORMED

Figure 1-8 A P-N junction with forward bias applied.

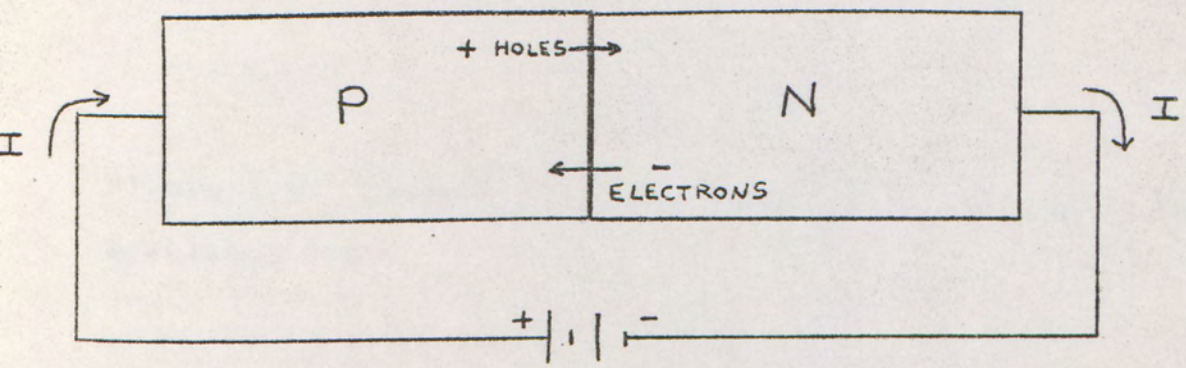

+ HOLES
P
N
I
I
ELECTRONS
+
-

Figure 1-9 Current flow as a function of applied voltage in a silicon diode.

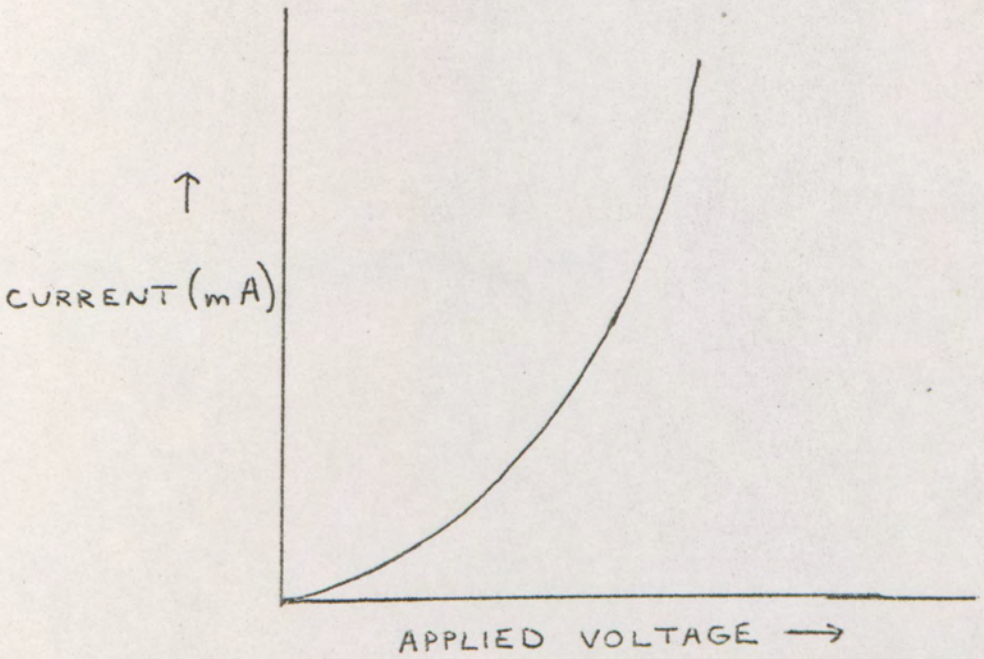
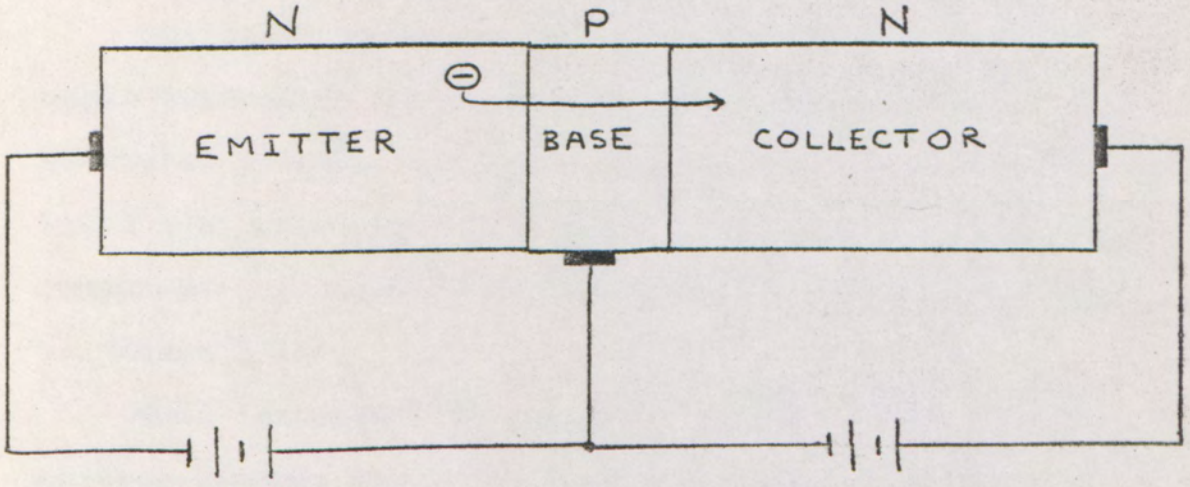

CURRENT (mA)
APPLIED VOLTAGE

Figure 1-10 An NPN transistor.

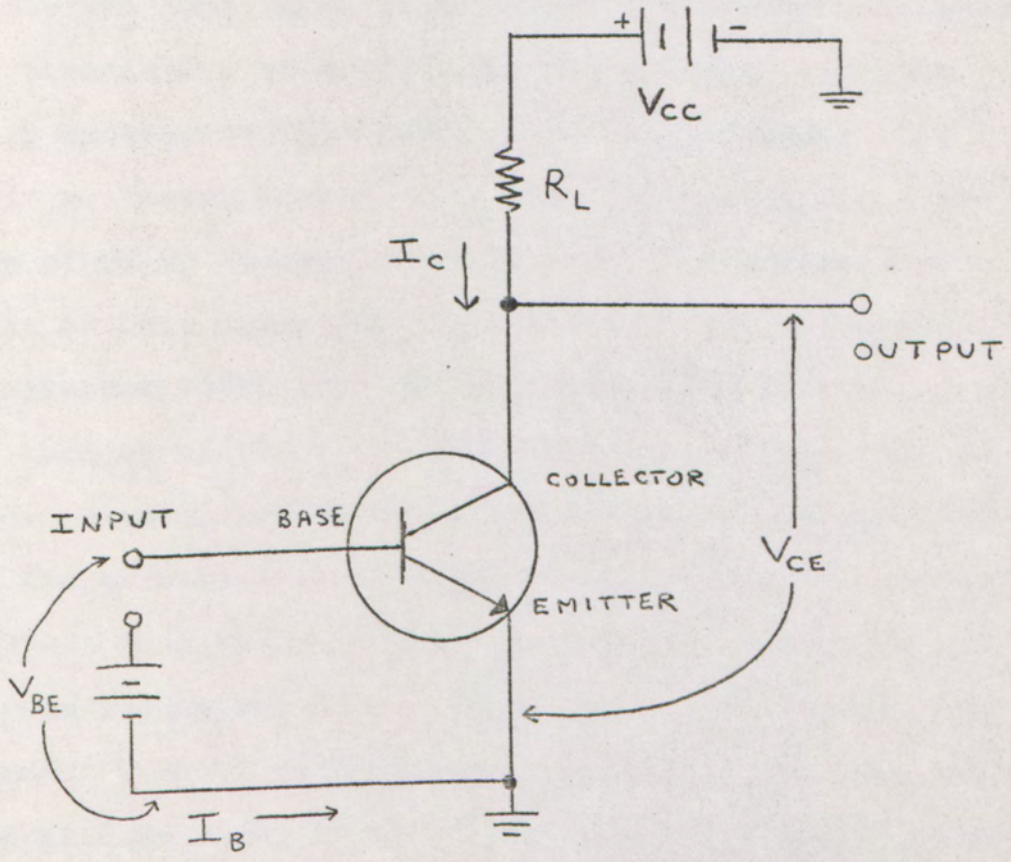

N
P
N
⊖
EMITTER
BASE
COLLECTOR

The transistor operates in the following manner: electrons leaving the emitter enter the base in search of holes to combine with. The extremely thin base, however, captures only about 2 percent of the total number of electrons entering it. The remaining 98 percent pass across the next P-N junction into the collector where the reverse bias of the externally applied potential pulls the electrons through the collector region and around the external circuit back to the emitter. Regulation of the small base current allows one to control the much larger collector current.

Our point of departure into the above discussion of basic transistor theory was the use of a transistor as a saturated switch, i.e., one which is either in a logic high level (on) or a logic low level (off). This is called the common-emitter circuit configuration[18]; and is illustrated in Figure 1-11.

When the potential difference between the base and the emitter exceeds 0.8 v the transistor will turn on fully, or in saturation. This voltage represents the junction breakdown potential. When in saturation the transistor's impedance between collector and emitter is very low and the amount of current flowing through the transistor is determined by the value of the load resistance, R_L[19]. I_C is then essentially V_{CC}/R_L by Ohm's law. The output voltage V_{CE} equals the amount of current flowing through the transi-

Figure 1-11 NPN transistor common emitter configuration.


+
-
V_{CC}
R_L
I_C
OUTPUT
COLLECTOR
INPUT
BASE
V_{CE}
EMITTER
V_{BE}
I_B

stor times its resistance, which during saturation is quite low. Therefore V_{CE} is typically around 0.1 v for a silicon transistor. When V_{BE} drops below the turn-on threshold the transistor turns off (develops a high impedance) and the voltage appearing at the output becomes V_{CC}.

The TTL logic type uses, as was previously mentioned, input transistors to perform the basic logic functions. A readily understood TTL circuit is shown in Figure 1-12[20].

If we assume that +5 v is present at both the A and B inputs of Q1 no current would flow in the base-emitter circuit of this transistor because they are equipotential. The collector voltage of Q1 would therefore be high which would turn on Q2 since its threshold voltage has been exceeded. With Q2 turned on in saturation the collector will be at the transistors saturation voltage level - around 0.1 to 0.3 v. Thus the output of the total gate will be low when both inputs are high. If either A and/or B are low (grounded) then Q1 will conduct, Q2 will be off, and the output will be high, or +5 v. The above gate performs the NAND logic function.

The output impedance of the circuit in Figure 1-12 changes depending on whether Q2 is conducting or not. This acts to slow the switching time of the logic network. The circuit illustrated in Figure 1-13 provides for much better performance for the output impedance is low even when Q4 is

Figure 1-12 A two input TTL NAND gate.

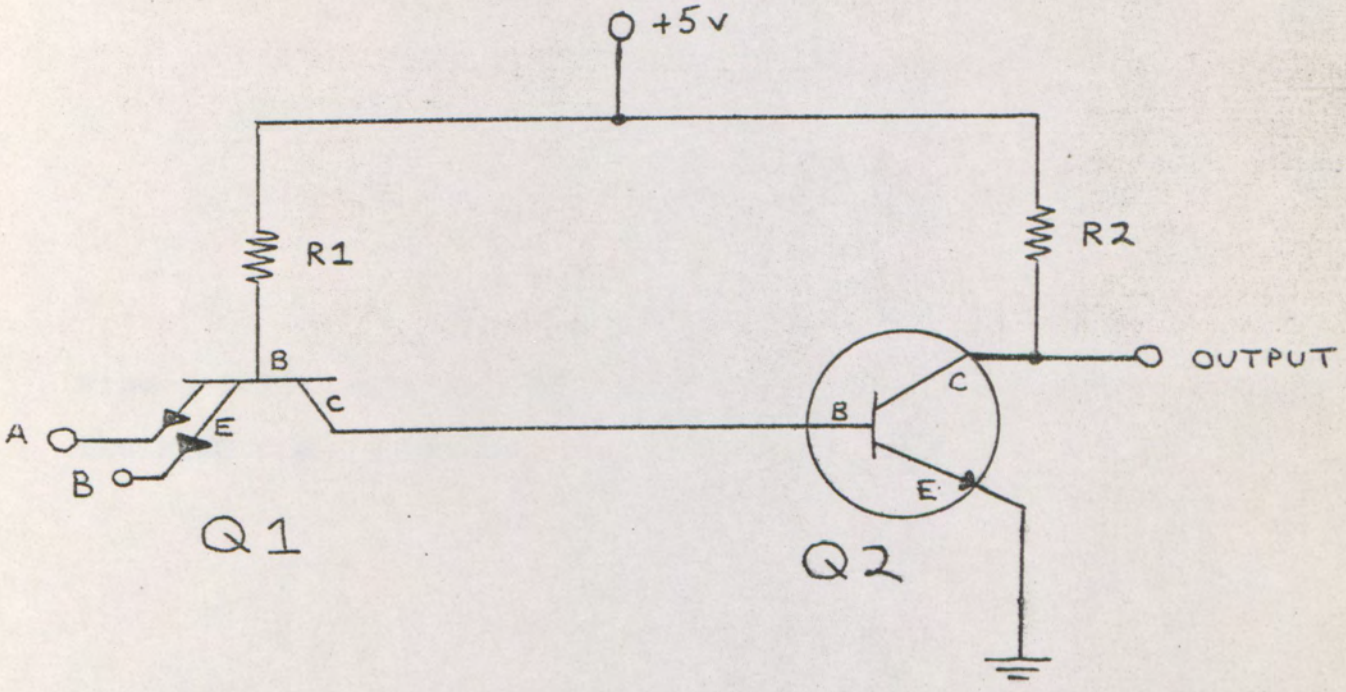
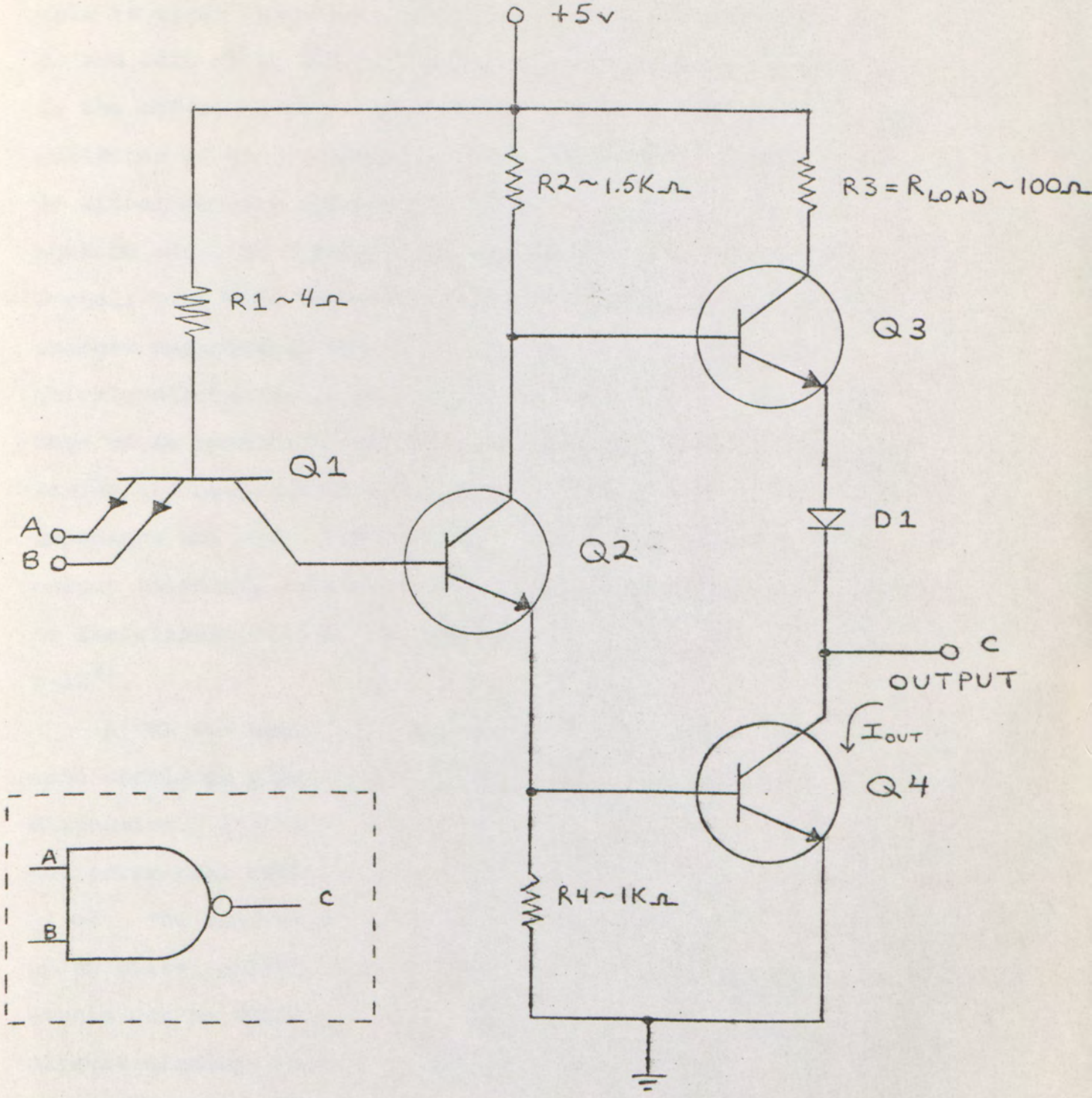

+5v
R1
R2
B
C
E
A
B
Q1
B
C
E
OUTPUT
Q2

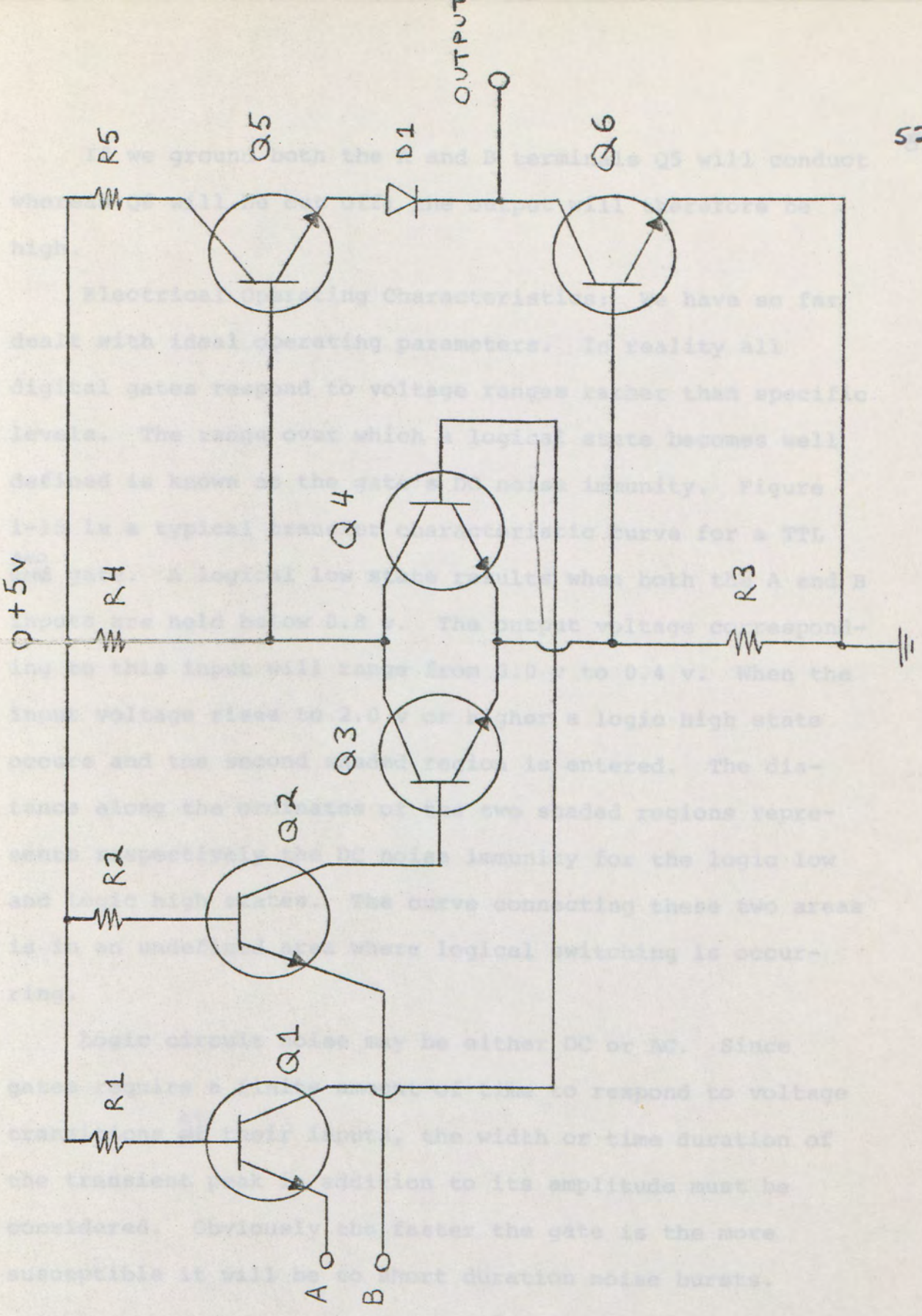
Figure 1-13 An improved TTL NAND gate; dashed portion contains the NAND logic symbol.


+5v
R2~1.5KΩ
R3 = R_LOAD ~ 100Ω
R1~4Ω
Q3
Q1
A
B
Q2
D1
C
OUTPUT
I_OUT
Q4
R4~1KΩ
A
B
C

nonconductive. Analysis of the circuit will demonstrate this is true. When both A and B are high the collector of Q_1 and base of Q_2 will be high. Q_2 will turn on holding Q_3 in the off state while turning Q_4 on; the output tied to the collector of this transistor will subsequently be held low. If either or both emitters of Q1 are low, Q2 and Q4 will both be off. Q3 however will conduct and the output of the overall gate will be high. Notice that when Q4 conducts any charged capacitance across the output (and ground) will quickly discharge through Q4 because of its low impedance. When Q4 is nonconducting Q3 is turned on and the capacitance across the output will decay through R_3, Q_3 and D_1 - a total impedance not very different than Q4 alone. Since the output impedance is essentially constant the operating speed of the circuit will be faster than the NAND gate of Figure 1-12[21].

A TTL NOR gate is presented in Figure 1-14. Its operation should be easily understood in light of the previous discussion. If the A input is high (equal to +5 v) only the collector-base circuit of Q1 will conduct, which will turn Q4 on. The emitter of Q4 will turn on Q6 with its high going pulse, pulling the output low. The same course of events can be traced when B is high, except the active circuit elements become Q2 and Q3. Note that at no time has Q5 been driven into conduction.

Figure 1-14 A TTL NOR gate.


OUTPUT
R5
Q5
D1
Q6
+5v
R4
Q4
R3
Q3
Q2
R2
Q1
R1
A
B

If we ground both the A and B terminals Q5 will conduct whereas Q6 will be cut off; the output will therefore be high.

Electrical Operating Characteristics: We have so far dealt with ideal operating parameters. In reality all digital gates respond to voltage ranges rather than specific levels. The range over which a logical state becomes well defined is known as the gate's DC noise immunity. Figure 1-15 is a typical transfer characteristic curve for a TTL ~~and~~ AND gate. A logical low state results when both the A and B inputs are held below 0.8 v. The output voltage corresponding to this input will range from 0.0 v to 0.4 v. When the input voltage rises to 2.0 v or higher a logic high state occurs and the second shaded region is entered. The distance along the ordinates of the two shaded regions represents respectively the DC noise immunity for the logic low and logic high states. The curve connecting these two areas is in an undefined area where logical switching is occurring.

Logic circuit noise may be either DC or AC. Since gates require a finite amount of time to respond to voltage transitions ~~of~~ at their inputs, the width or time duration of the transient peak in addition to its amplitude must be considered. Obviously the faster the gate is the more susceptible it will be to short duration noise bursts.

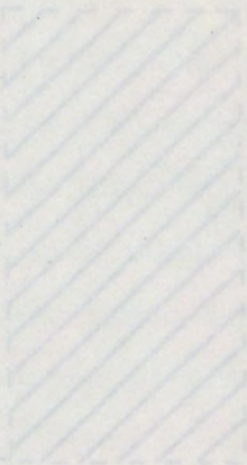
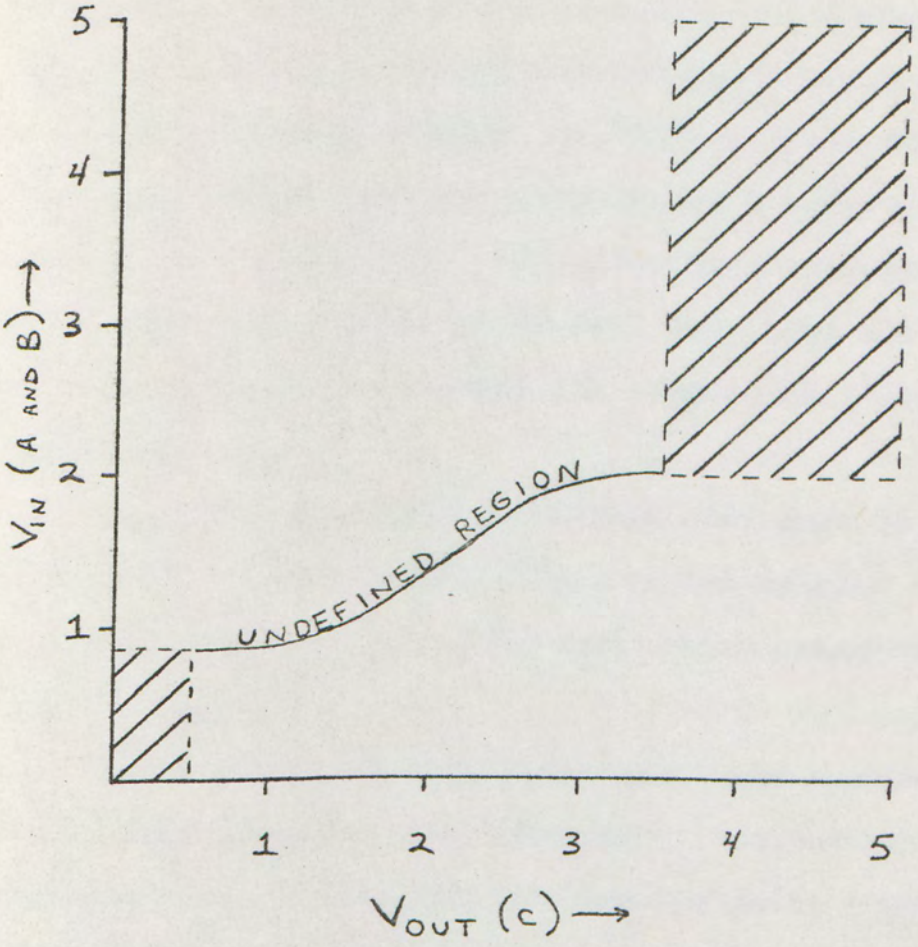
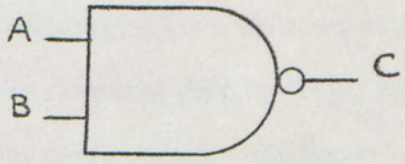


Figure 1-15 Transfer characteristic curve for typical AND gate.


5
4
3
2
1
V_{IN} (A AND B) →
UNDEFINED REGION
1
2
3
4
5
V_{OUT} (C) →


A
B
C

The speed of a logic device is usually defined in terms of gate propagation delays and maximum operating frequencies. A propagation delay is the time it takes a gate to respond to a valid voltage transition at its input. For TTL circuits the value is typically below 50 nano-seconds.

The maximum operating (switching) frequency is that frequency above which the gate can no longer track and change its output accordingly. TTL gates have maximum operating frequencies of from 20 to 50 MHz, but there are high speed emitter coupled gates which can respond to frequencies as high as 350 MHz.

One final operating parameter that must be mentioned is "fan-out"[22]. This defines the current driving capability of a particular gate; i.e., how many other gates may be driven from its output.

Other operating parameters exist and can be found in the various manufacturer's handbooks and performance sheets[1]; those mentioned above are the factors which commonly need to be considered in design work.

Complex Logic Elements: Up to now we have concentrated our analysis on the TTL circuit. One reason for doing so which has not been mentioned, is that most applications of medium scale integration (MSI) technology have utilized TTL. An MSI circuit is generally defined as one which contains

---

1 See Appendix 1 for Data Sheets.

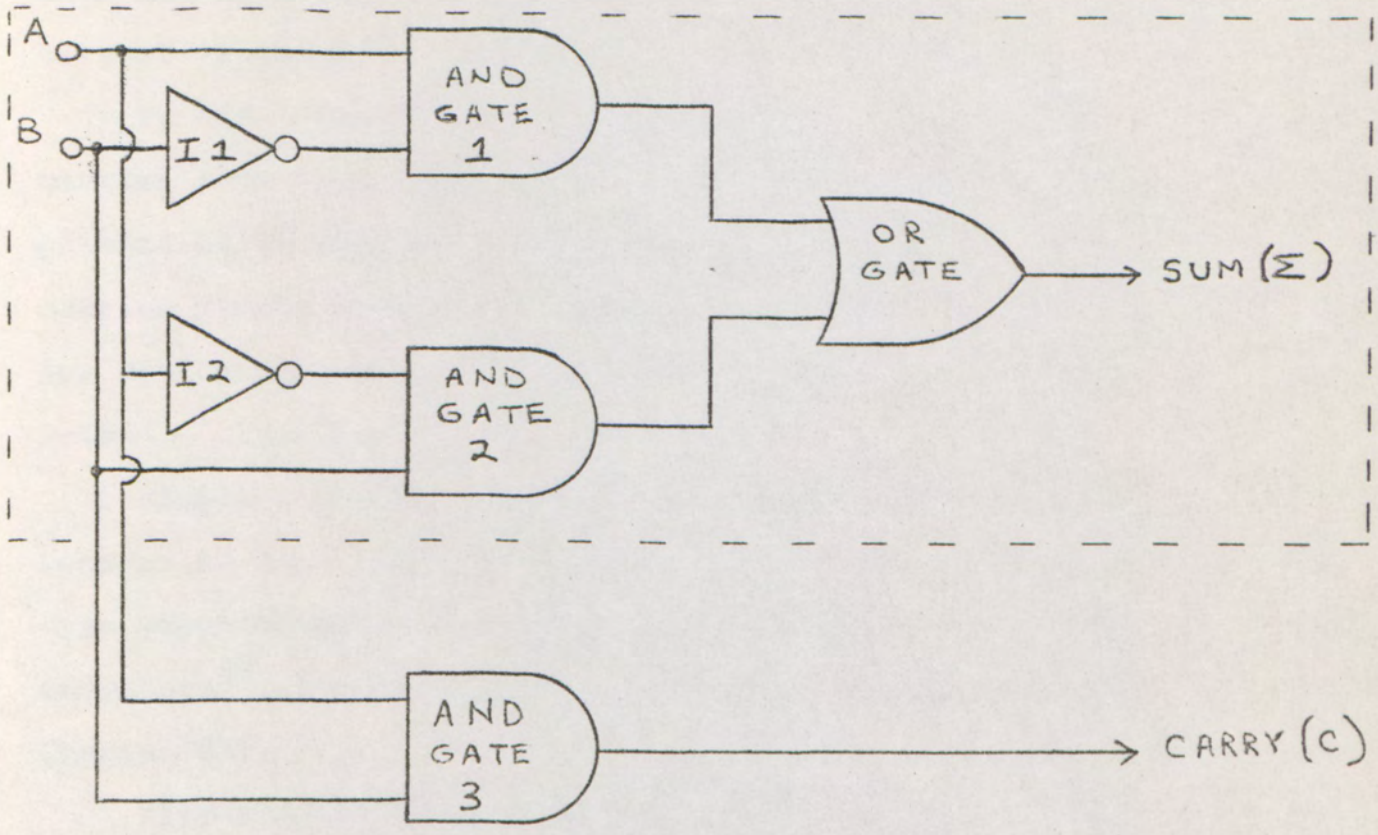
from 30 to 100 gates per chip. Thus our narrow view will be a benefit in the examination of more complex digital logic packets.

Adders: In digital computers counting operations are performed in binary. All computer arithmetic is based on addition and subtraction: multiplication is accomplished through multiple addition, and division through repetitive subtraction. Since digital logic states are defined as either on or off, high or low signal, etc., knowledge of the binary number system is needed, (for a good review see Reference 23). Because large binary numbers are cumbersome a short hand notation that uses base 8 is commonly employed: $011\ 010\ 111\ 101_2 = 3275_8$[24].

In digital computers gates are hooked together to form adding circuits. Figure 1-16[25] is the circuit for a half-adder which can add two binary numbers and also indicate that both inputs A and B are 1 by executing a carry. The truth table in the figure illustrates the result of four possible input combinations. When both A and B are low 1/2 of AND gates 1 and 2 are high because of invertors I_1 and I_2: but that is not enough to turn on these gates, so the outputs are both 0. However when either A or B is 1 one of the AND gates will conduct and Σ will equal 1.

When both A and B are equal to 1 a carry will result as AND gate 3 will be turned on; the summation output will be 0.

Figure 1-16 Half adder and its truth table.



A	B	Σ	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The outlined portion in Figure 1-16 is itself the binary adder. It is commonly called the EXCLUSIVE-OR function and an alternate representation for the half-adder circuit is shown in Figure 1-17[26].

To add larger binary numbers together requires that carries from lower stages be accounted for. This is accomplished by hooking together half-adders in such a way that carries ripple from stage to stage as they occur. A simple two bit[1] binary ripple carry adder is presented in Figure 1-18.

Ripple carry full-adders are available as discrete IC packets in 2, 4, or 8 bit capabilties. It is IC's of this type which comprise the arithmetic section of most digital computers[27], (see discussion of Altair 8800 Microprocessor, Chapter II).

Flip-Flops: Logic decisions and the results of addition must often be placed in a temporary memory system either for future manipulation or to keep track of computation. An important logic circuit which fulfills this need is the flip-flop, a bistable multivibrator capable of being utilized as a digital on-off switch, temporary data latch, shift register (temporary data storage device) and event counter.

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1 BIT is to binary as digit is to decimal.

Figure 1-17 Alternate symbolic representation of half adder.

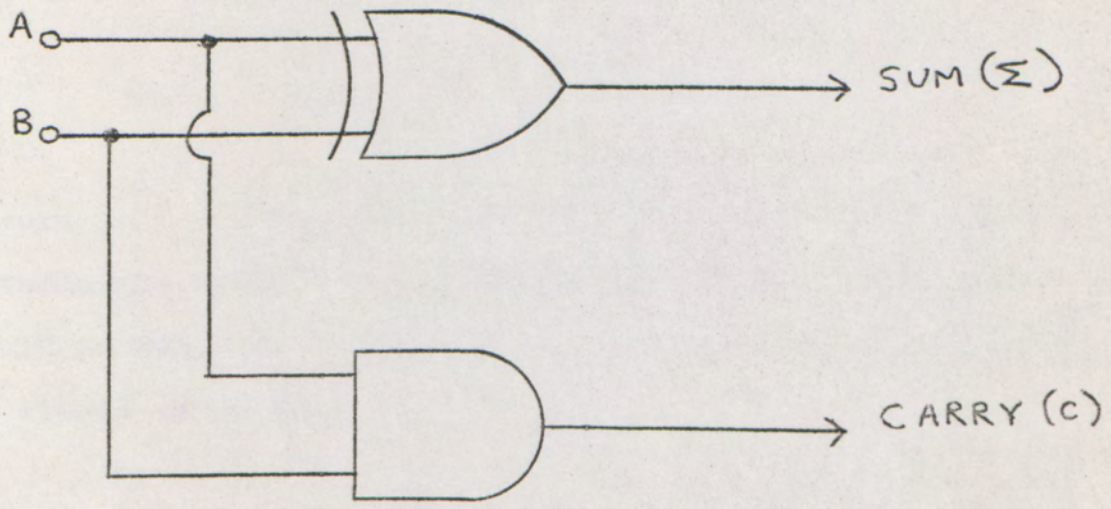
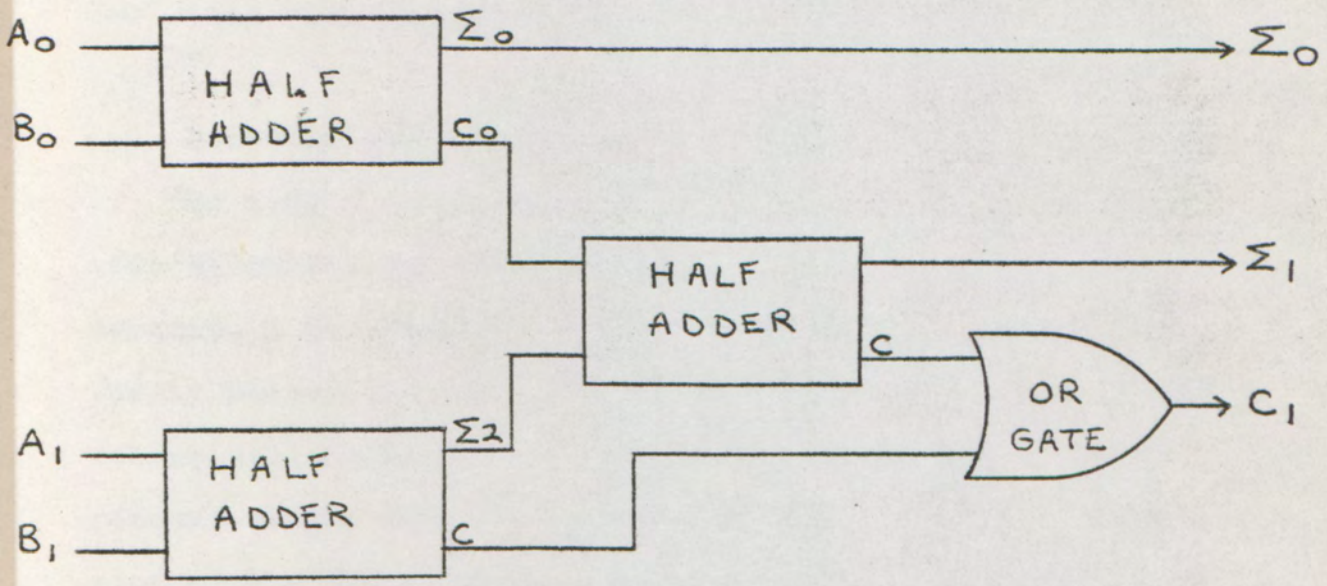

A
B
SUM (Σ)
CARRY (C)

Figure 1-18 A two bit binary ripple carry adder. Boolean algebra notation is used; a (+) indicates an OR operation, whereas what would normally be considered as a multiplication operation should be viewed as an AND.



$$C_0 = A_0 B_0$$

$$\Sigma_0 = A_0 + B_0$$

$$\Sigma_1 = A_1 + B_1 + C_0$$

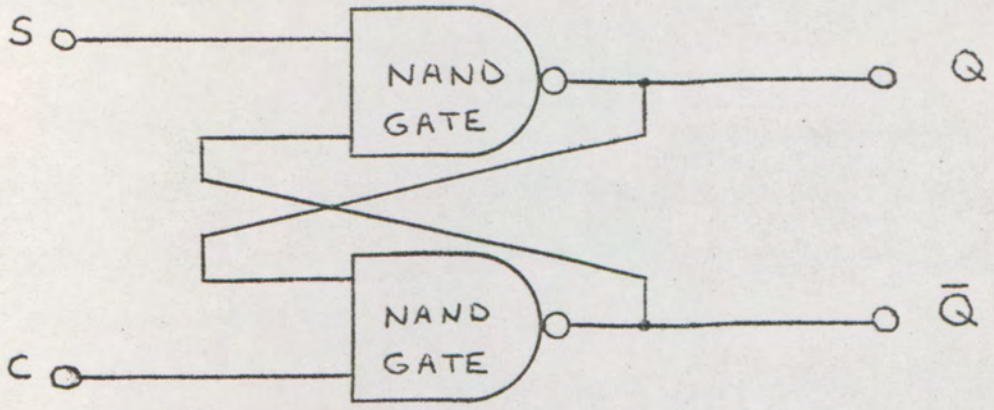
$$C_1 = A_1 B_1 + \Sigma_2 C_0$$

The simplest flip-flop is the reset-set, RS, flip-flop. It is a device which has two stable states and which will remain in one of the two states until a pulse is applied to one of the inputs. The operation of the flip-flop is most easily understood if it is considered to be constructed from two cross coupled NAND gates, as is illustrated in Figure 1-19[28].

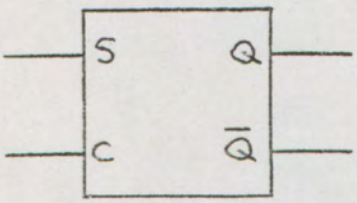
Consider the situation when the S and C inputs are both 1. The output Q may be either a 1 or a 0, the only stipulation at this point is that the $\overline{Q}$ and Q outputs be complementary, i.e., when $\overline{Q}$ = 1, Q = 0, etc. Now if S is momentarily pulsed with a low going signal (held to ground) the Q output will become a 1 and therefore $\overline{Q}$ will go to 0 independent of the previous condition of the outputs. Examination of the truth table in Figure 2-4 for a NAND gate will indicate why this is so; only when both inputs to a NAND gate are high is the output low.

Accordingly when C input is held low momentarily, the $\overline{Q}$ output goes to a 1 regardless of its previous state. The flip-flop will remain in this state until the inputs are once again pulsed, thus serving as a binary data storage device. The truth table for the RS flip-flop is also given in Figure 1-19. It should be noted that time is now a factor: t_n being the time before the specified input conditions have been applied, and t_{n+1} being the time after S and C have been set to specific values.

Figure 1-19 An RS flip-flop: (a) constructed from cross coupled NAND gates; (b) block diagram for an RS flip-flop; (c) truth table for the RS flip-flop.



(a)



(b)

CASE #	INPUTS S	INPUTS C	t_n Q	t_{n+1} Q	t_{n+1} $\bar{Q}$
1	1	0	X	0	1
2	0	1	X	1	0
3	0	0	X	UNDEFINED	UNDEFINED
4	1	1	X	NO CHANGE	NO CHANGE

(c)

t_n = TIME BEFORE SPECIFIED INPUT CONDITIONS APPLIED

t_{n+1} = TIME IMMEDIATELY AFTER CHANGE

X = EXISTING STATE DOES NOT MATTER

The R-S flip-flop however will enter an undefined state when both inputs are low thus making it essentially useless for counting operations[29]. It can still be used as a data storage latch, a device specifically designed for the temporary storage of binary information.

For counting operations a clocked flip-flop must be employed (see Figure 1-20). When the S and C inputs are used the outputs will change only when a negative going pulse enters the clock input, T. This is called synchronous mode. However there is still an undefined state when all gated inputs are equal to 1. This is resolved by hooking the flip-flop in JK mode as shown in Figure 1-21, a modification which prevents the condition where all inputs equal 1.

If C_1 and S_2 are connected together and connected to a binary 1, then every other time the clock input is negatively pulsed the Q output (and consequently $\overline{Q}$) will change. Thus the flip-flop only changes output after it has counted 2 input pulses. Hence the J-K flip-flop is ideally suited as the building block of counters[1], (see Figure 1-22).

---

1 Because of critical timing requirements two J-K flip flops are usually hooked in what is known as a master-slave configuation; this provides for much higher noise immunity as well as less critical timing. Almost all commercially available clocked F-F's are of the master-slave type[31].

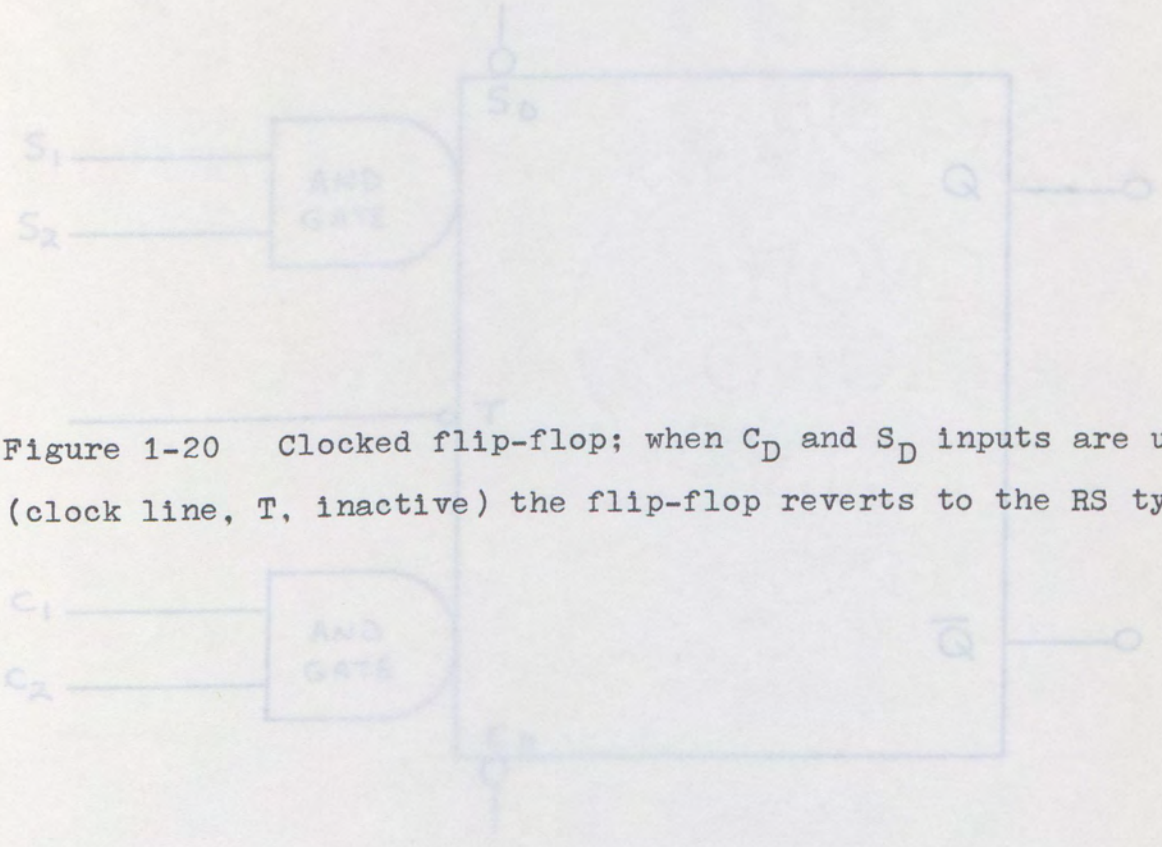


Figure 1-20 Clocked flip-flop; when C_D and S_D inputs are used (clock line, T, inactive) the flip-flop reverts to the RS type.

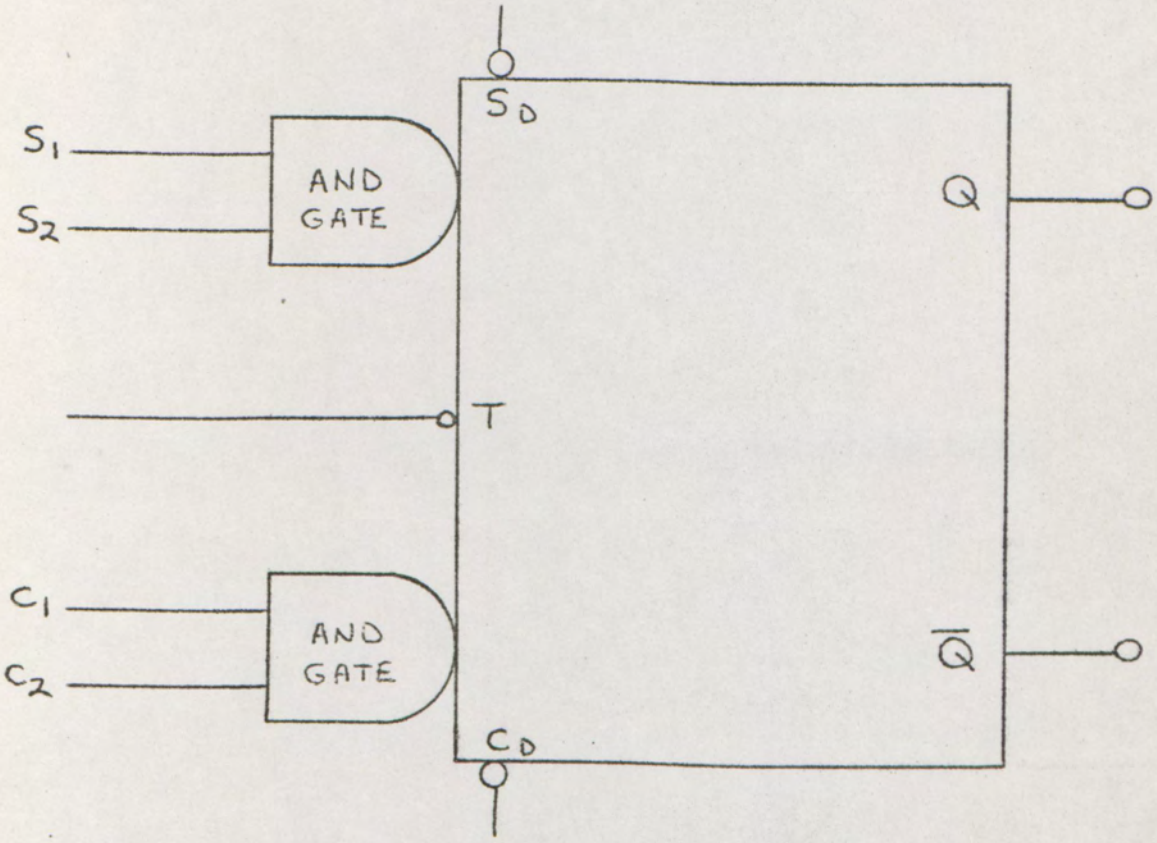
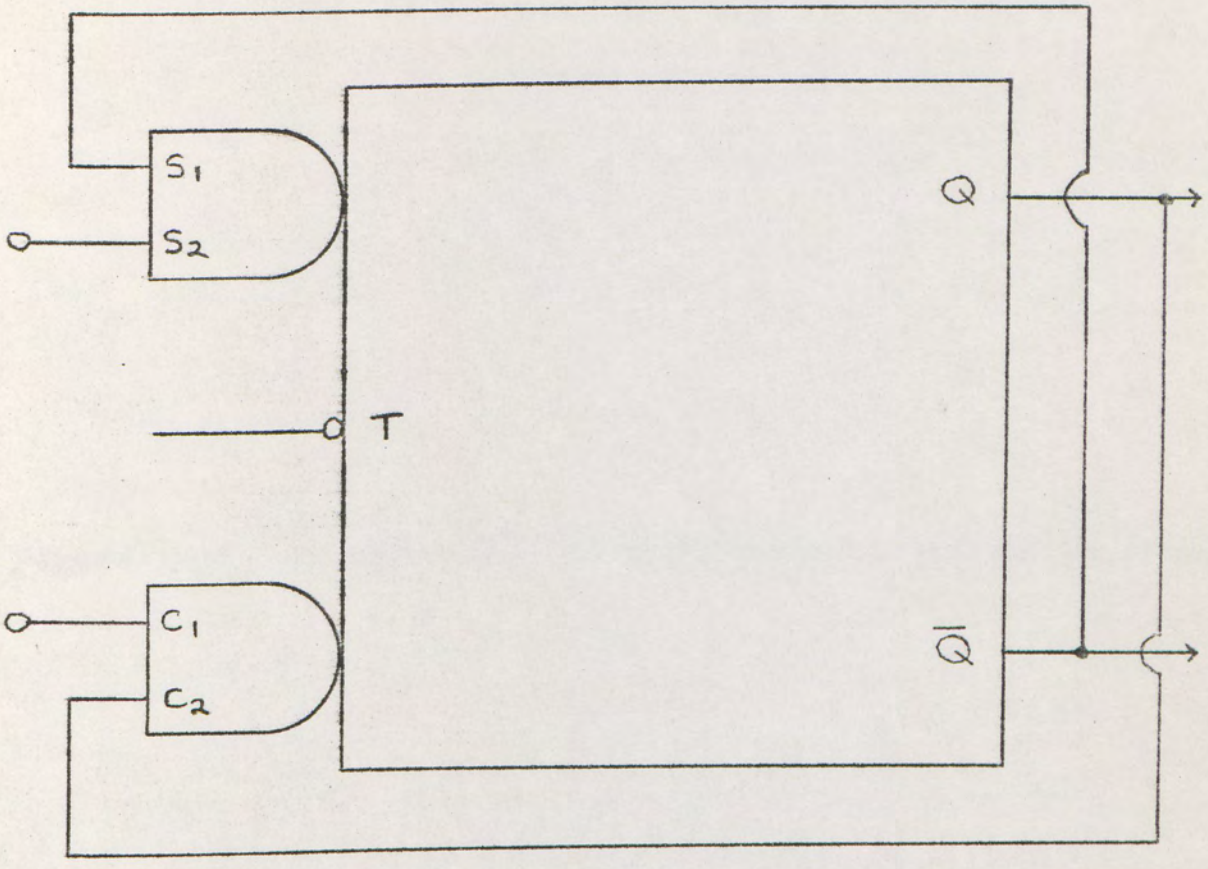
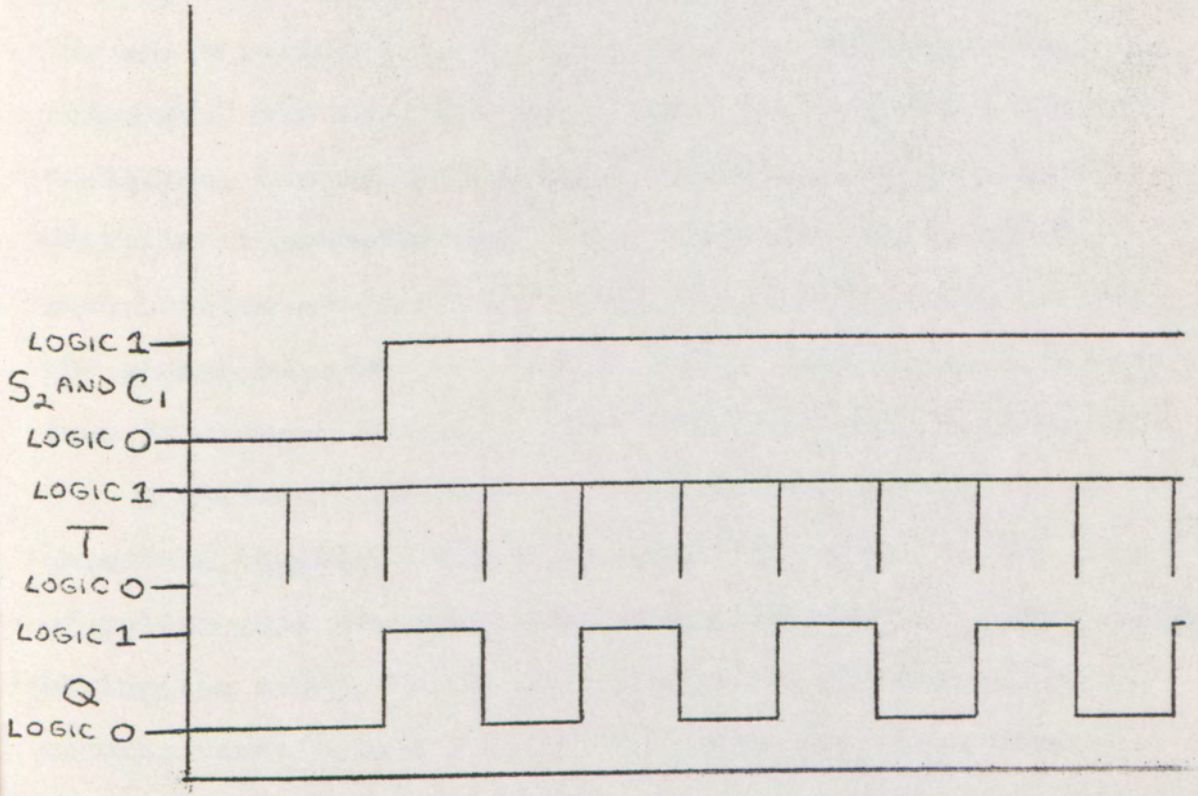

S_1
S_2
AND GATE
S_D
Q
T
C_1
C_2
AND GATE
$\overline{Q}$
C_D

Figure 1-21 JK flip-flop and associated truth table.



t_n		t_{n+1}	
S_2	C_1	$\bar{Q}$	Q
0	0	NO CHANGE	NO CHANGE
1	0	1	0
0	1	0	1
1	1	COMPLE	MENTARY

Figure 1-22 Timing chart for JK flip-flop connected as a counter.


LOGIC 1
S_2 AND C_1
LOGIC 0
LOGIC 1
T
LOGIC 0
LOGIC 1
Q
LOGIC 0

The J-K flip-flop is the building block from which the shift register is constructed. Shift registers like data latches are used for data storage. However unlike data latches they can input and output information in either serial or parallel form. (In parallel transmission all elements of a digital word are available simultaneously; serial transmission causes one bit of a word to be available at a specific time, the way a typewriter presents data[30].) The shift register is an integral component of digital computers, for in addition to the above mentioned characteristics, the device can move data within the register while it is being stored[2]; many basic machine language instructions interact with registers of this type to test the status of a memory location or an input/output device, (see discussion of Altair 8800 I/O structure, Chapter II).

Counters: Counters are an important element in an interface circuit. They provide for determining the number of pulses that have appeared at a clock input on the chip by having the states of the flip-flops, which make up the counter, continuously available as outputs. Thus event counting, sampling rate specification and frequency division may be accomplished by this device.

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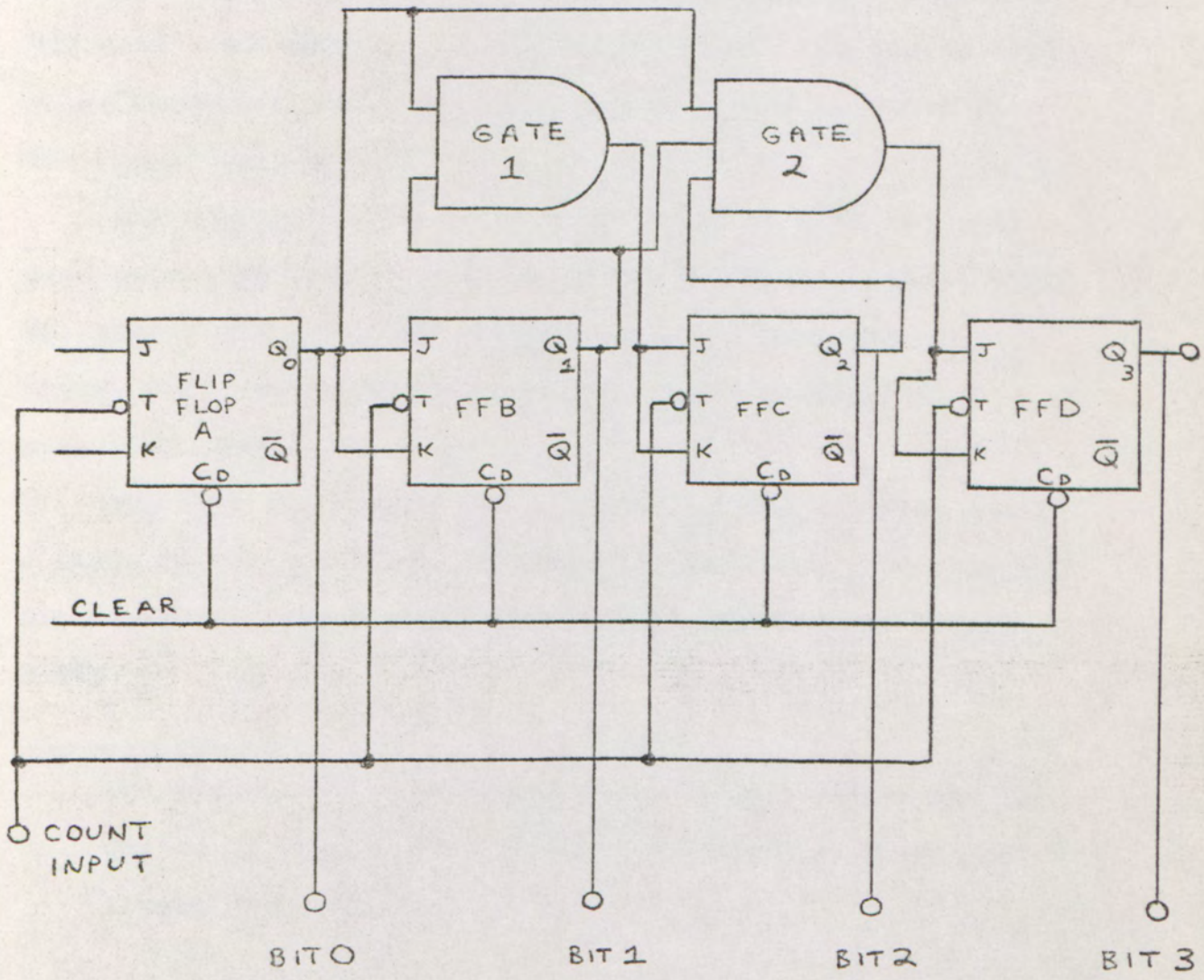
1 For further information see Reference 14, pg. 165-169.

There are two types of counters available: asychronous and synchronous. The former is the simpler of the two accomplishing its function by rippling counts from flip-flop to flip-flop[32]. One soon realizes that this system has a distinct disadvantage. Since counts ripple from one stage to the next, propagation delay times will become significant as the total number of flip-flops in the counter increases. Output counting spikes are also an inherent fault of the asynchronous counter. These problems add up to low noise immunity and slow operating speeds, because the maximum count rate is determined by the total propagation delay of the flip-flops[33].

An alternative to the asynchronous mode of counting is the synchronous counter of Figure 1-23. It is constructed from J-K type flip-flops and two AND gates; it will count up from 0 to 15_{10} in binary. Since the two external gates set up the J-K inputs of the last two flip-flops only the propagation delays of one flip-flop (FFA) and the gates need be considered. Thus the synchronous counter can operate at much higher speeds as well as without output counting spikes[34].

The counter in Figure 1-23 operates as follows: a pulse is applied to the clear line which sets all flip-flops to 0. The first low going pulse on the clock line will change the output of FFA (Q_o) from a 0 to a 1; no other

Figure 1-23 A synchronous binary up counter.


GATE 1
GATE 2
J
T
K
FLIP FLOP A
FFB
FFC
FFD
CLEAR
COUNT INPUT
BIT 0
BIT 1
BIT 2
BIT 3

flip-flops outputs will be affected because the J-K inputs on FF(B,C,D) are all initially at logical 0. The high output of FFA will enable the clock input of FFB by holdings its J-K inputs at a logical high level. Thus when the second clock pulse occurs FFA will go to 0 while FFB's output will become 1. Two clock pulses have thus far occured, and the output is $10_2 = 2_{10}$ as it should be. The third clock pulse causes Q_o and Q_1 to equal 1[1]. This sets the clock input of FFC by providing the necessary inputs to AND gate 1 so that its output can go high. The fourth clock pulse changes Q_2 to a logical 1 while Q_0 and Q_1 go to 0. The output is now $100_2 = 4_{10}$.

The counter in Figure 1-23 can also be made to count down merely by reading data from the $\overline{Q}$ outputs instead of Q. The timing chart for the above counter is presented in Figure 1-24; it is the same as that for an asynchronous binary up counter.

The type of counter that is used in the external sweep portion of the interface (see Chapter II) is a synchronous 4 bit binary up/down counter with preset inputs (see Figure 1-25).

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1 See Figure 1-22 - remember that 2 clock pulses are required to change the output of a flip-flop whose J-K inputs are tied high.

Figure 1-24 Timing chart for synchronous binary up counter.

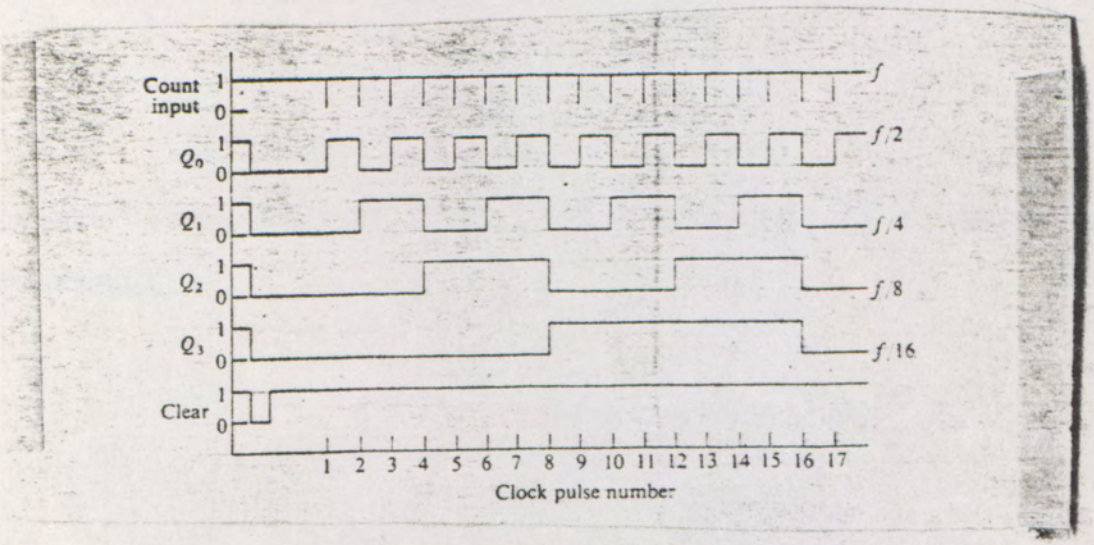
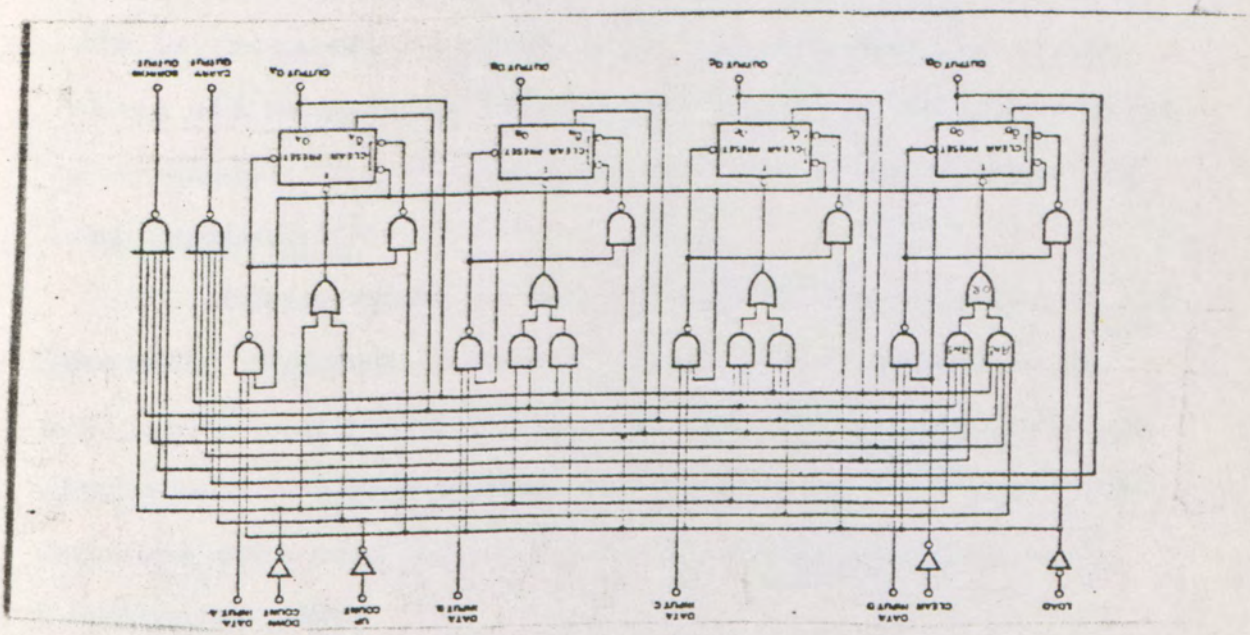

Count input
1
0
f
Q_0
f/2
Q_1
f/4
Q_2
f/8
Q_3
f/16
Clear
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
Clock pulse number

Figure 1-25 Logic diagram for the N74193 synchronous up/down counter.



The direction of counting is determined as follows: to count up the up input is pulsed while the down input is held high. Counting down is accomplished in a similar manner by pulsing the down counter while the up input is held high.

The counter is entirely programmable in that the output may be preset to any desired value. A low going pulse to the load line will enter whatever values are present at the data inputs into the counter, independent of the count pulses, and hold the counter at that value until the load line is released. A clear input is also provided which forces all outputs to logic level 0 when a low going pulse is applied. This input is independent of both count and load inputs.

To obtain counts of higher than 15 these counters are specially designed so that they may be cascaded with no additional logic circuitry. The mode of cascading is the ripple borrow/carry method, as illustrated in Figure 1-26. Counters connected in this manner are operating in semi-synchronous mode.

The borrow output produces a pulse equal in width to the count down input pulse when the counter outputs all become equal to 0. Similarly when the counter is full (all outputs = 1) the next clock pulse will cause a pulse equal in width to the clock to appear at the carry output. The timing chart for this counter is presented in Figure 1-27.

Figure 1-26 Synchronous binary counters connected in ripple carry/borrow cascade mode to provide semi-synchronous operation.

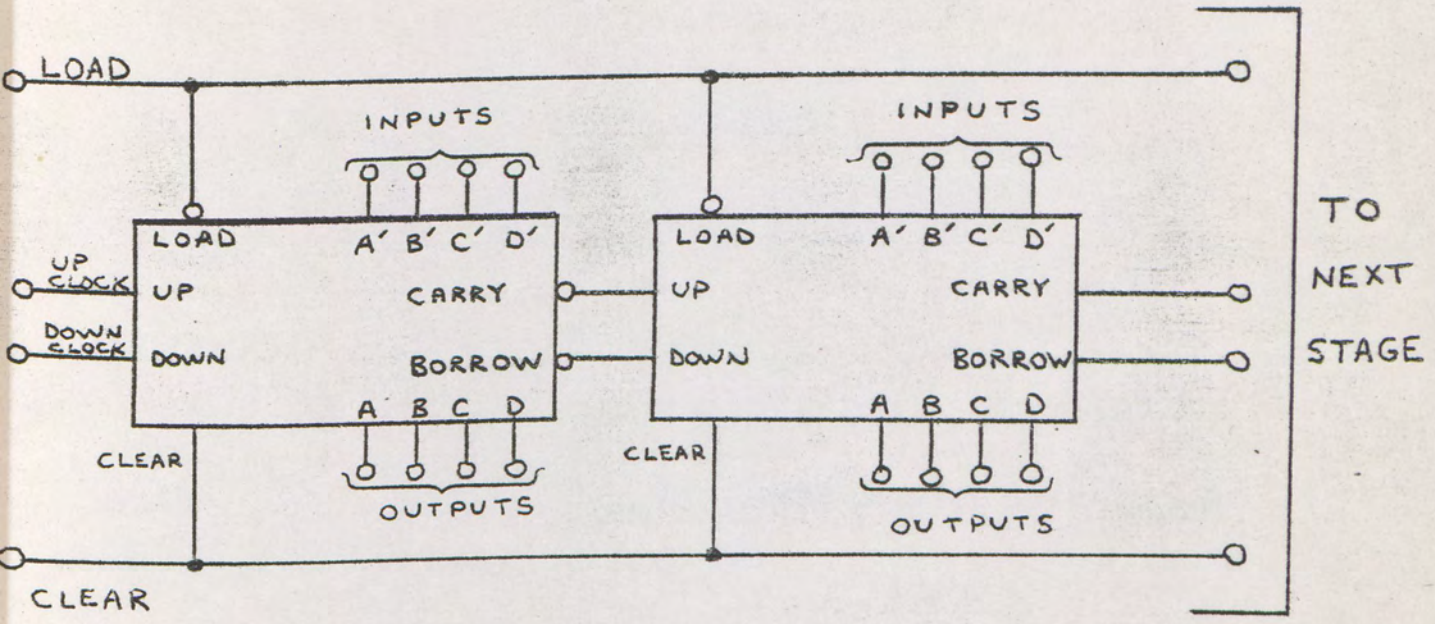
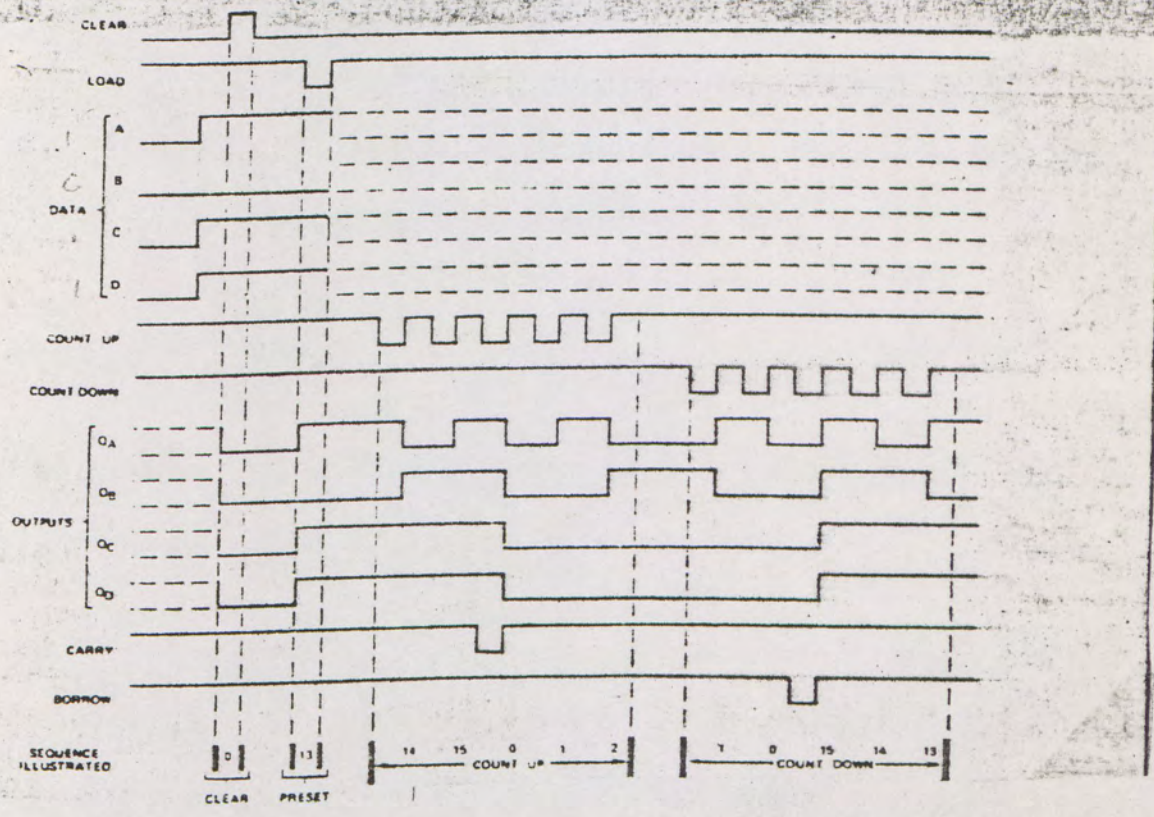

LOAD
INPUTS
INPUTS
LOAD
A' B' C' D'
LOAD
A' B' C' D'
UP CLOCK
UP
CARRY
UP
CARRY
DOWN CLOCK
DOWN
BORROW
DOWN
BORROW
A B C D
A B C D
CLEAR
CLEAR
OUTPUTS
OUTPUTS
CLEAR
TO NEXT STAGE

Figure 1-27 Timing chart for N74193 counter with typical sequence illustrated.

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to ~~BCD seven~~ 13.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



Digital to Analog Converters: The digital to analog converter is an electronic packet which accepts digital information and in turn provides as an output a continuously variable analog signal which is a function of the digital information. The necessity of such a device is due to our need to have information in real world form: Abstract numbers which are difficult to deal with are converted to an analog signal. The output of D/A converters may be used to drive meters, sound alarms, trigger an oscillosope display, run a chart recorder, modulate waveforms, or serve as precision power supply, (see Figure 1-28).

The basic D/A provides a current output which is inversely proportional to the digital input. By Ohm's law the amount of current flowing in the circuit is:

$$I_{TOTAL} = \frac{V_{REF.}}{R_{TOTAL}} \qquad \text{Eqn. 1-8}$$

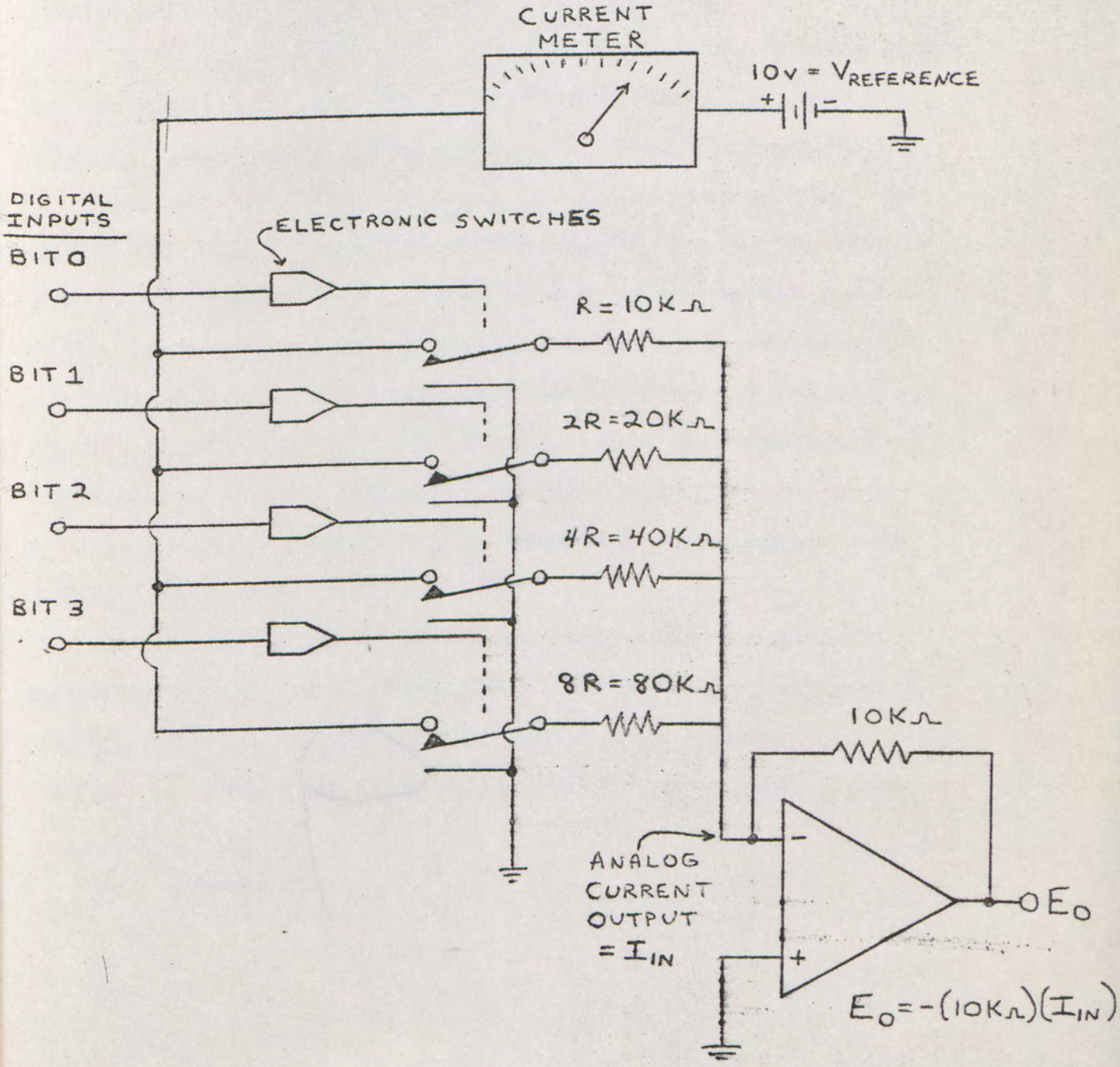
With only S_1 closed (binary 1 appearing at BIT^0 input) the total current will be:

$$I_{TOTAL} = \frac{10\ v}{10K\Omega} = 1\ mA \qquad \text{Eqn. 1-9}$$

When S_4 is closed and all other switches open:

$$I_{TOTAL} = \frac{10\ v}{80K\Omega} = 0.125\ mA \qquad \text{Eqn. 1-10}$$

Figure 1-28 Simple four bit digital to analog converter; all switches shown in the on position.


CURRENT METER
10v = V REFERENCE
+
-
DIGITAL INPUTS
ELECTRONIC SWITCHES
BIT 0
BIT 1
BIT 2
BIT 3
R = 10K Ω
2R = 20K Ω
4R = 40K Ω
8R = 80K Ω
10K Ω
ANALOG CURRENT OUTPUT = I_{IN}
E_o
$E_o = -(10K\Omega)(I_{IN})$

Thus when S_1 is closed the current, I, is inversely proportional to 2^0, and when S_4 is closed the current is inversely related to 2^3 or 8. In this way each switch adds a binary weighted increment of current to the operational amplifier's summing input. The negative output voltage is directly related to this input current and thus to the original binary code that appeared at the D/A inputs[36].

It is interesting to note that other number systems can be represented by the output of the D/A merely by changing the magnitude relationship between the precision resistors.

The D/A used in the external sweep portion of the interface (see Section III of this report) is the DAC-10Z-3, a low cost bipolar general purpose analog to digital converter manufactured by Analog Devices Inc[1]. It features 10 bit resolution and a maximum linearity error of $\pm$ 1/2 LBS, ($\pm$ .05% of full scale). The time required for conversion is a maximum of 5 micro seconds. Internal reference voltage stabilization is provided by a temperature compensated zener diode, (see Figure 1-29).

Analog to Digital Converters: The analog to digital converter is the translation element between the real world and the abstract binary representation that computers must deal with. Less than 15 years ago this type of data trans-

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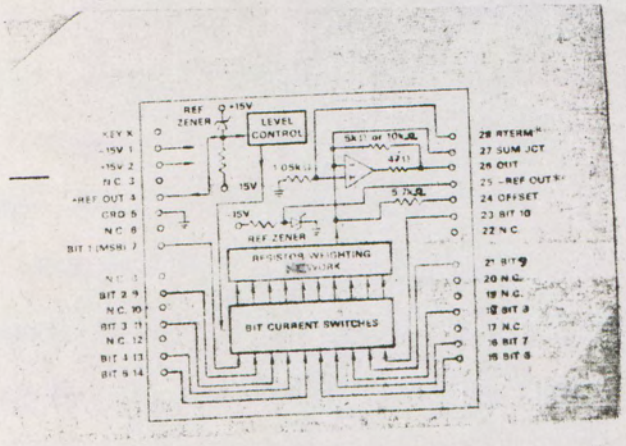
1 See Appendix 1.

Figure 1-29 Block diagram of DAC-10Z D/A converter.

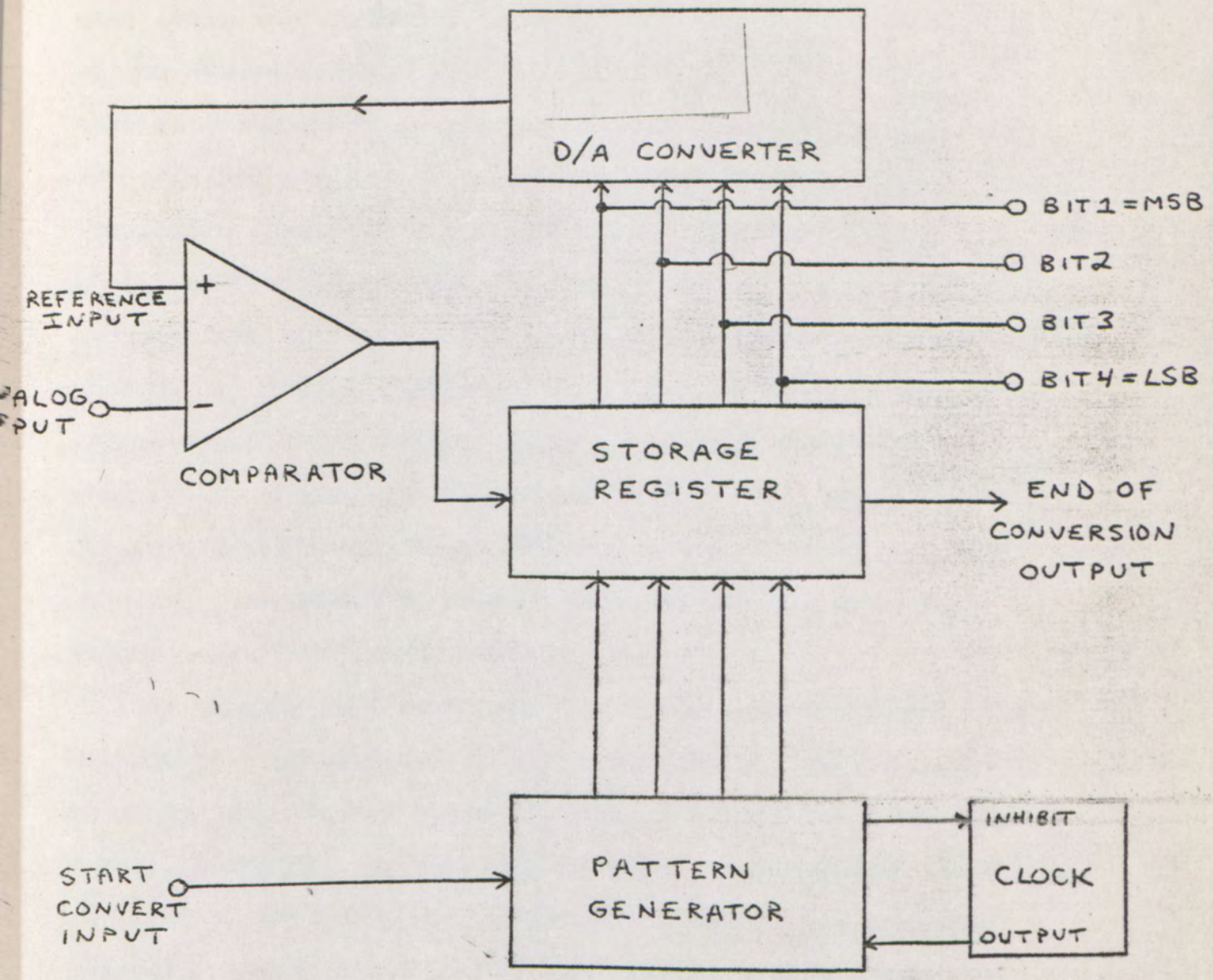

REF ZENER
+15V
LEVEL CONTROL
5kΩ or 10kΩ
42Ω
1.05kΩ
15V
5.7kΩ
-15V
REF ZENER
RESISTOR WEIGHTING NETWORK
BIT CURRENT SWITCHES
-KEY X
-15V 1
+15V 2
N.C. 3
+REF OUT 4
GRD 5
N.C. 6
BIT 1 (MSB) 7
N.C. 8
BIT 2 9
N.C. 10
BIT 3 11
N.C. 12
BIT 4 13
BIT 5 14
28 RTERM*
27 SUM JCT
26 OUT
25 -REF OUT*
24 OFFSET
23 BIT 10
22 N.C.
21 BIT 9
20 N.C.
19 N.C.
18 BIT 8
17 N.C.
16 BIT 7
15 BIT 6

lation was a tricky, and quite expensive, proposition. A/D converters capable of 50,000 sample/second conversion rates consumed 500 watts of electrical energy cost about $8000, and their dimensions measured in feet; today equivalent devices sell for under $1000 and require only a few hundred milli-amps of current to operate. MSI has allowed for both the price and size reduction[37].

There are many types of A/D converters available to the designer today; the most widely used type, however, is the successive-approximation A/D. Its desirable features include high resolution, high speed of conversion, and compatability with computer interfaces. Although high conversion rates were not a requirement of the NMR to computer interface, (since data sampling rates are not very great) maximum flexibility in the converter's usefulness for other more demanding interfacing problems was the determining factor in purchasing this type of converter.

A typical A/D converter is illustrated in Figure 1-30. Notice that this system contains a comparator, a device which accomplishes just what its name suggests. It is an analog device with two inputs, one of which is a reference, the other is some analog input signal. When the input signal rises above the magnitude of the reference supply the output of the comparator changes from a digital logic high to a low state. The output changes back when the input signal falls below the voltage value of the reference.

Figure 1-30 Four bit successive approximation A/D converter.


D/A CONVERTER
BIT 1 = MSB
BIT 2
BIT 3
BIT 4 = LSB
REFERENCE INPUT
+
ALOG PUT
−
COMPARATOR
STORAGE REGISTER
END OF CONVERSION OUTPUT
START CONVERT INPUT
PATTERN GENERATOR
INHIBIT
CLOCK
OUTPUT

A positive going pulse into the start convert input will cause the converter to begin the digital approximation of the analog input. This method is quite similar to the chemist's system of precisely weighting an unknown quantity. The A/D compares a set of "n" binary weighted voltages to the analog input for the comparator. More precisely, the start convert pulse frees the control logic clock which becomes free running. This causes the pattern generator to produce an initial binary number output of 1000_2. This word is converted to an analog signal by the D/A converter portion of the system and fed to the comparator. Before the internal clock produces another pulse the most significant bit (MSB) has been compared to the analog input and found either to be too "heavy" or too "light"[38].

If the MSB is larger than the analog input voltage then the MSB will be switched off by the leading edge of the next clock pulse. If it is smaller, than a 1 will remain in the storage register. During the lifetime of the second clock pulse bit 2 is forced to a logical 1 state by the pattern generator, and the sum of the MSB and bit 2 will enter the comparator. The new output state of the comparator will, when gated by the next clock pulse, instruct the storage register to keep or discard that bit. This process is continued until the LSB has been evaluated; when this has been completed an end of conversion pulse is provided to

signal that the word present at the digital output is valid. An example will clarify the procedure.

All of the possible number combinations that can be generated by the pattern generator of a 4 bit successive approximation converter are presented in Figure 1-31.

It will be noted that for a 4 bit A/D of the approximating type, four steps are always required for complete conversion. Thus the conversion rate is constant.

Suppose that an input voltage equal to a binary output value of 9_{10} appears at the analog input part of the comparator. The converter will load 1000_2 or 8_{10} into the D/A and compare the MSB with this analog signal. Since the value of the analog signal is the greater of the two, the MSB will be "locked" into the storage register.

The number $1100_2 = 12_8$ will be transferred to the comparator reference input upon the next clock pulse. Since this number is larger than the signal input, bit 2 is made a 0 in the storage register. 1010_2, the next number to appear at the comparator, is also too large; therefore the storage register places a 0 in the bit 3 position. The next clock pulse causes 1001_2 to be compared to 9_{10} at the analog input; since they are equal the 1 is latched into the LSB position of the storage register. The valid digital equivalent of this sequence is illustrated by the dashed portion of Figure 1-31[39]. At the end of the conversion the digital

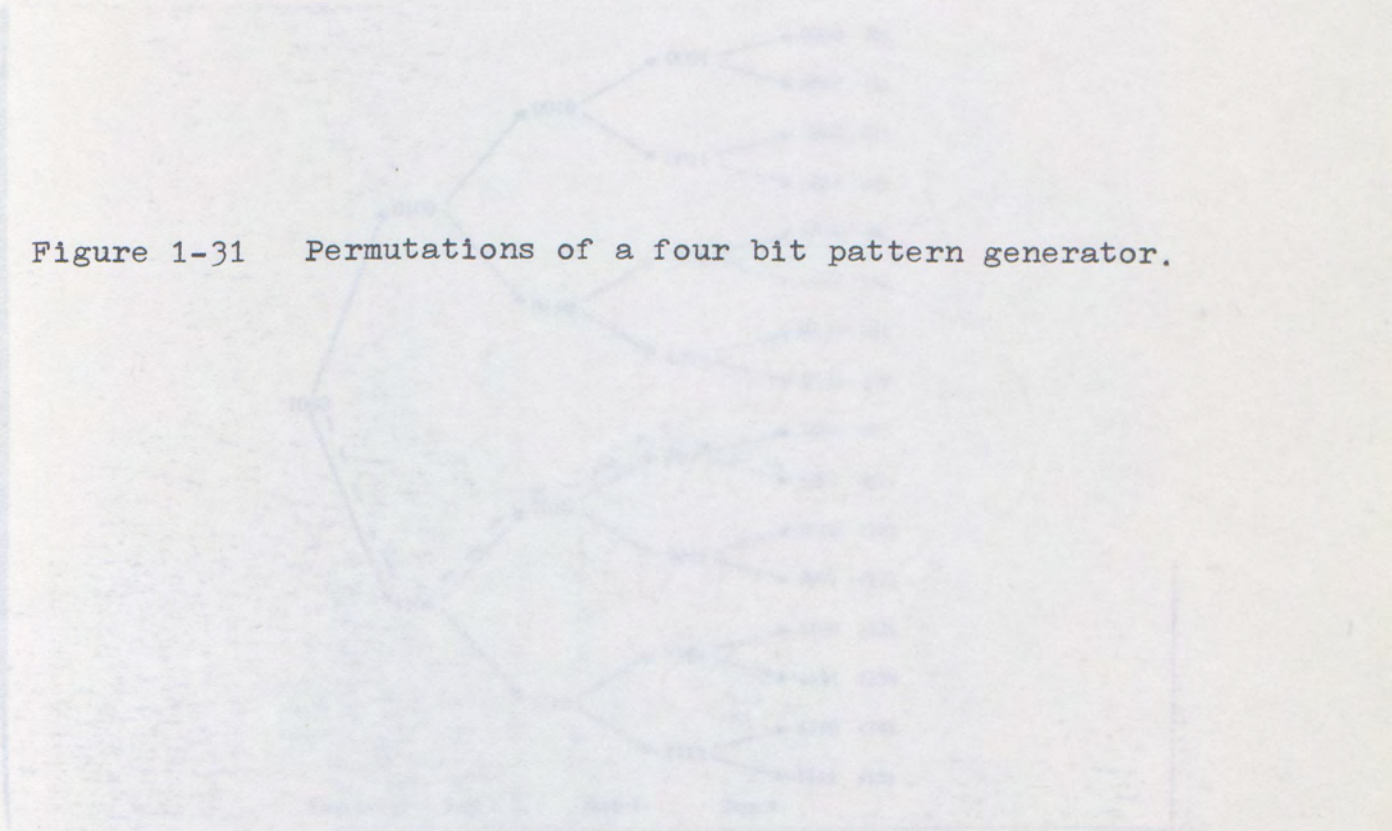
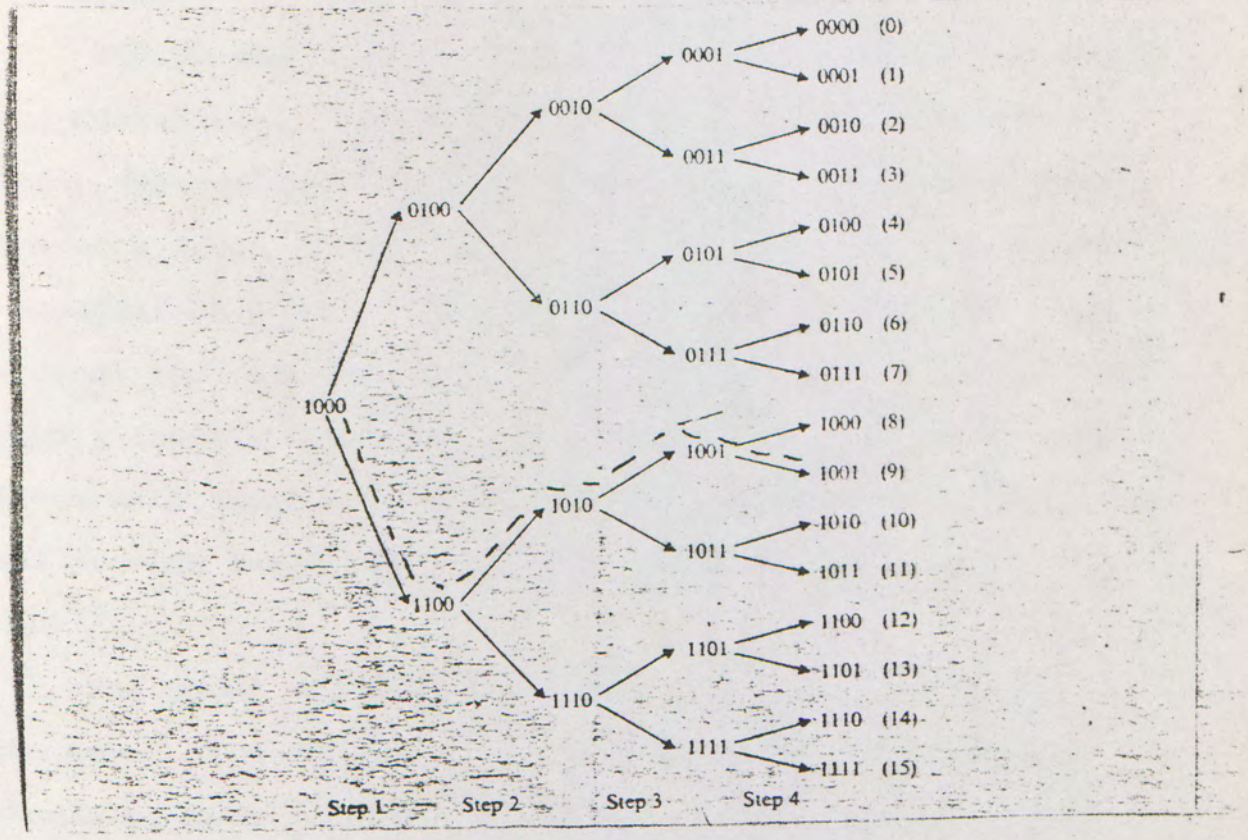


Figure 1-31 Permutations of a four bit pattern generator.



9_{10} = INPUT VOLTAGE = 1001_2

equivalent of the analog signal input is made available at the digital output parts of further processing.

The signal portion of the electronic interface (see Chapter II) uses DATEL SYSTEMS' MODEL ADC-EH8B1 8 bit analog to digital converter. Its fast conversion rate (4.0 micro seconds) and low cost made it ideally suited for our purposes; Figure 1-32 is a functional block diagram of the converter[1].

Wiring and Interconnection Parameters for Digital Logic and Converters: Noise (see Section A) is the "enemy" of logic systems; and the faster the response time of a gate the more prone it will be to noise induced timing and synchronization error. The main guidelines to minimize noise include the decoupling of every logic package from its power supply input to ground using a 0.1 μF capacitor. The capacitors will shunt high frequency power supply noise to ground and provide large instantaneous current demands when necessary[40].

The power supply must be well regulated and stable in the event of heavy transient current demands. AC ripple should be held to within 5 percent of the supply voltage[41].

Grounding is also extremely important. Separate grounds should be avoided because of the likelihood of ground loop formation. This problem causes various system

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1 See Appendix 1 for complete specifications

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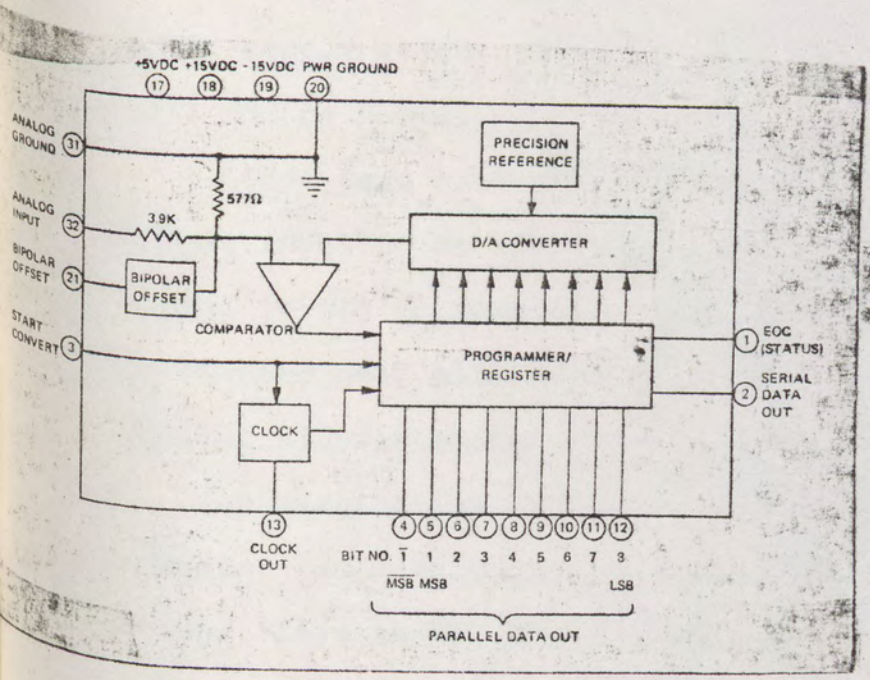
1 See Appendix 1 for complete specifications

Figure 1-32 Eight bit A/D converter model ADC-EHB by Datel Systems Inc.



FAST, 8 BIT ANALOG TO DIGITAL CONVERTER

MODEL ADC-EH8B

grounds to be at different potentials relative to one another thus increasing DC noise levels, as well as increasing the impedance of the ground line. A system ground "mecca", where all ground lines are run to, will help alleviate these problems. This mecca should be placed near the power supply ground and runners to it should be as wide as possible.

If more than one board is incorporated into the system, power supply input wires to these boards should be as large as possible to reduce lead inductances; decoupling of the logic supply at the entrance point on the board to ground will reduce noise.

Converters have some additional requirements. The signal input to an A/D should be kept as far away from logic signal levels as possible. The converter itself should not be located near motors, relays or transformers. Analog and digital signals should not be run parallel.

An examination of Figure 1-32 indicates two different grounds: an analog and a power supply ground. Separate ground lines should be run from these terminals to the mecca point. This is done to minimize ground potentials that supply currents, analog signals and logic gate return currents would create if they were to flow through a common ground line[42].

Long distance (more than a few feet) transmission of low level analog signals should be avoided where possible.

A/D converters should be located at their inputs and D/A converters should be placed at the load. If long distance signal runs are unavoidable shielded cable, differential amplifiers and line drivers may have to be employed.

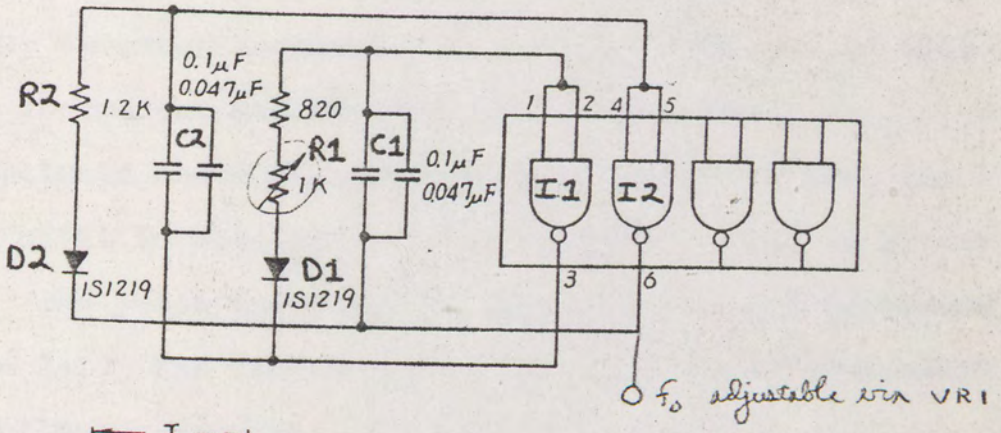
CHAPTER II

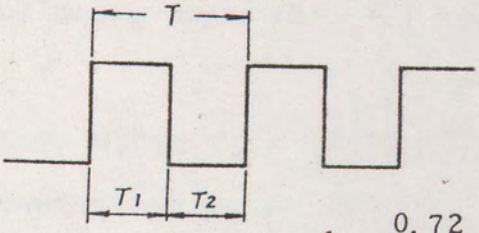
THE INTERFACE AND MICROPROCESSOR

A. TIME BASE MODULE

The heart of any computer linked data acquisition system is its time base or clock. The oscillator used to generate a stable time base in our application is illustrated in Figure 2-1[44]. The two inputs of the NAND gates are tied so that they perform the inversion function. For the purposes of explanation let us assume that the output of inverter 1 has just gone high. Capacitor C2 will act as a short circuit at the switching time of the inverter putting a logic one at the input of inverter 2, thus causing its output to go low. With the output of inverter 2 low current will flow through R2 and D2. Capacitor C2 will eventually

Figure 2-1 NAND gate clock pulse oscillator.





$T_1 = 0.693\ C_1R_1$ $\quad C_1 = C_2$

$T_2 = 0.693\ C_2R_2$ $\quad R_1 = R_2$

Provided $T = T_1 + T_2$

$= 0.693\ (C_1R_1 + C_2R_2)$

$= 0.693 \times 2\ (C_1 \cdot R_1)$

$$f_0 = \frac{0.72}{T} = \frac{0.72}{0.693 \times 2\ (C.R)}$$

$$= \frac{7200}{3.98} = 1.8\text{kHz}$$

stop the flow of charge; but R2 and D2 have bled off the positive charge at the input of I2 thus causing it to go low and, therefore, the output of I2 to become high.

Current flow from the output of inverter 2 has to occur through C1, which initially acts as a short circuit thus placing a logic one at the input of inverter 1. The output of this inverter switches from 1 to 0 and D1 and R1 will begin to conduct current from C1 to relative ground. But, as mentioned above capacitor C1 will charge causing the input of I1 to once again go low and its output to switch high. The pulse generated by this circuit is illustrated in Figure 2-1. The width of the timing pulses is determined by the following formula:

$$\text{GATE WIDTH } T_1 = .693\ C_1R_1$$
$$\text{GATE WIDTH } T_2 = .693\ C_2R_2 \qquad \text{Eqn. 2-1}$$

For a symetrical circuit where $R_1 = R_2 = R$ and $C_1 = C_2 = C$, provided that $T = T_1 + T_2$ then $T = 1.38\ RC$[45]. Because of the non-ideality of the square waves produced the frequency of switching is not exactly equivalent to the inverse of the period, T, but by the following relation:

$$f_o = \frac{0.72}{T} = \frac{0.72}{(0.693)(2)(RC)} \qquad \text{Eqn. 2-2}$$

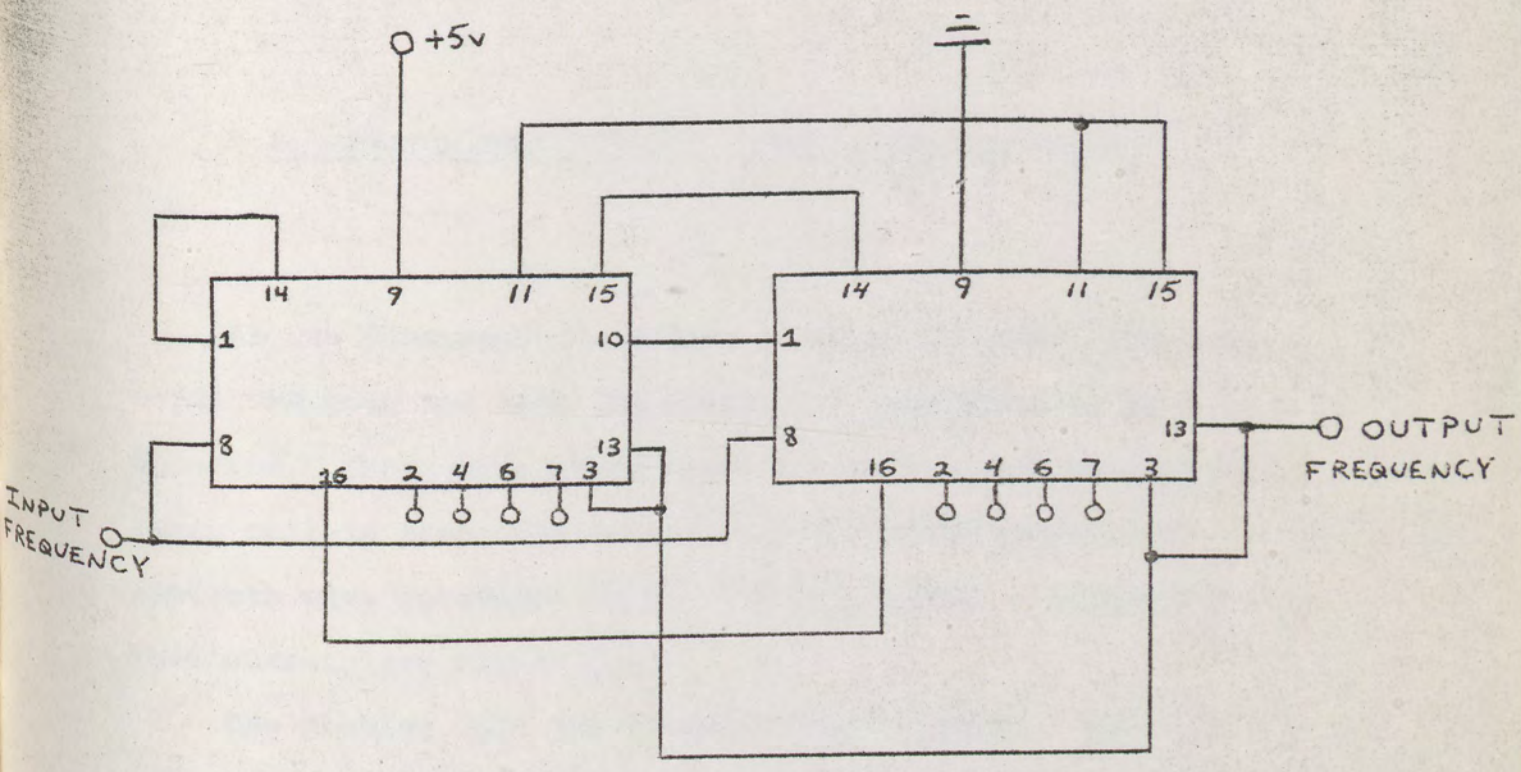
For the circuit as shown in Figure 2-1

$$f_o = \frac{7200}{3.98} = 1.8 \text{ K Hz} \qquad \text{Eqn. 2-3}$$

when the variable resistance, R1, is made equivalent to the fixed resistance, R2[46]. Frequency adjustment is obtained by varying the resistance of R1. The frequency of our square wave network has been set to 1696 Hz. The required frequency of clock pulses necessary to cause our external sweep generator to exactly duplicate the sweep time of the NMR is 26.5 Hz. Frequency division of the 1696 Hz is accomplished by modulo-n dividers. Our circuit employs National Semiconductor's DM8520 a single MSI chip containing over 50 gates. It can be programmed without external components to divide by any number from 2 to 15. When cascaded these dividers can be set for division by as large a number as one needs. The theory of operation and internal wiring of the chip may be found in Appendix 1. The connections for two dividers is illustrated in Figure 2-2. The cascading of two of these counters will allow for division by any number from 2 to 255 merely by holding certain of the P inputs to a logic level high, and others to a logic low, (see Figure 2 in the description of the DM8520 contained in Appendix 1).

The output from pin 6 of the 7400 NAND gate oscillator is fed to the input line on both of the divide by n chips.

Figure 2-2 Cascade mode connections for modulo-divide-by-n counters.



P1 = SERIAL INPUT
P2 = P1
P3 = SERIAL/PARALLEL INPUT
P4 = P2
P5 = Vcc
P6 = P13
P7 = P4
P8 = INPUT FREQUENCY
P9 = EX-OR CONTROL
P10 = SERIAL OUTPUT
P11 = 0000 DETECT
P12 = GROUND
P13 = OUTPUT FREQUENCY
P14 = EX-OR OUTPUT
P15 = EXT. EX-OR INPUT
P16 = PRESET

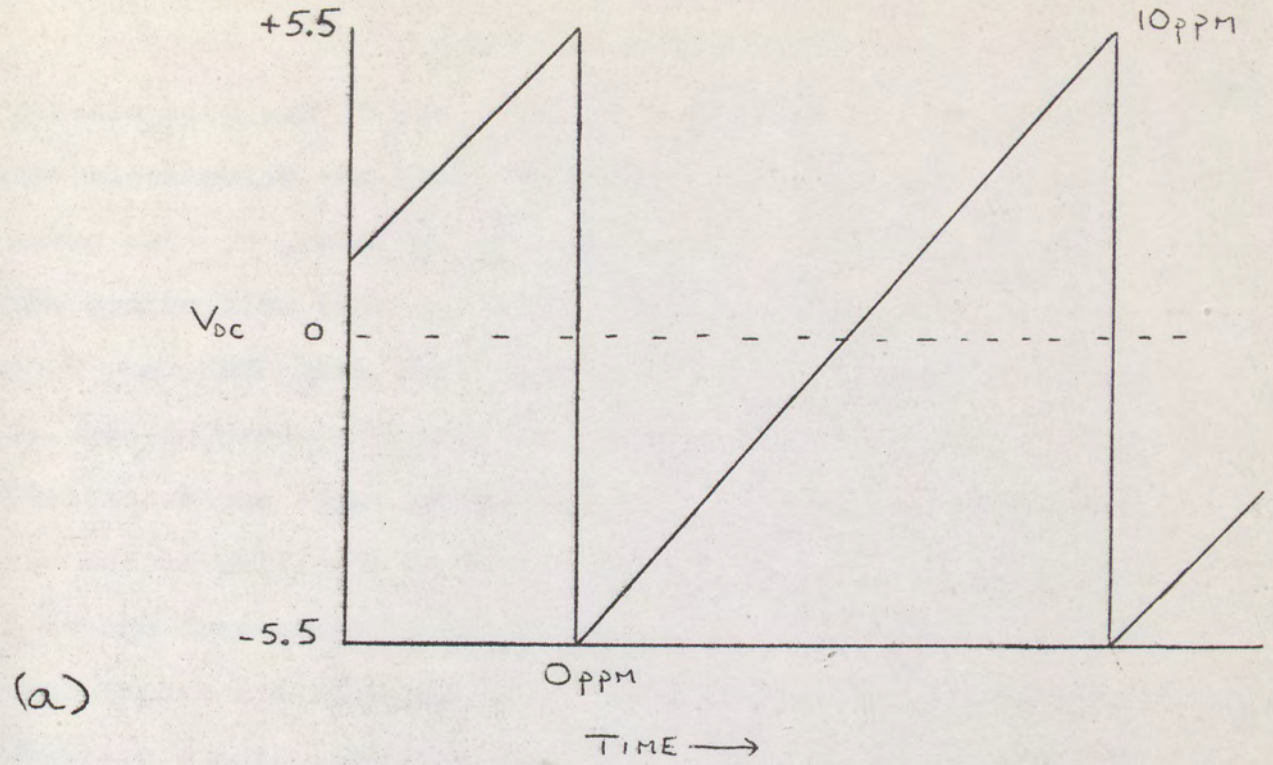
The P inputs on the chips have been set to divide by 64 so that the output frequency at pin 13 of the second divider is the 26.5 Hz that is required by the sweep generator. This clock rate is also used as the start convert command on the analog to digital converter, as will be explained in greater detail in the section on the ADC portion of the interface.

B. SWITCH DEBOUNCE AND SWEEP GENERATOR MODULE

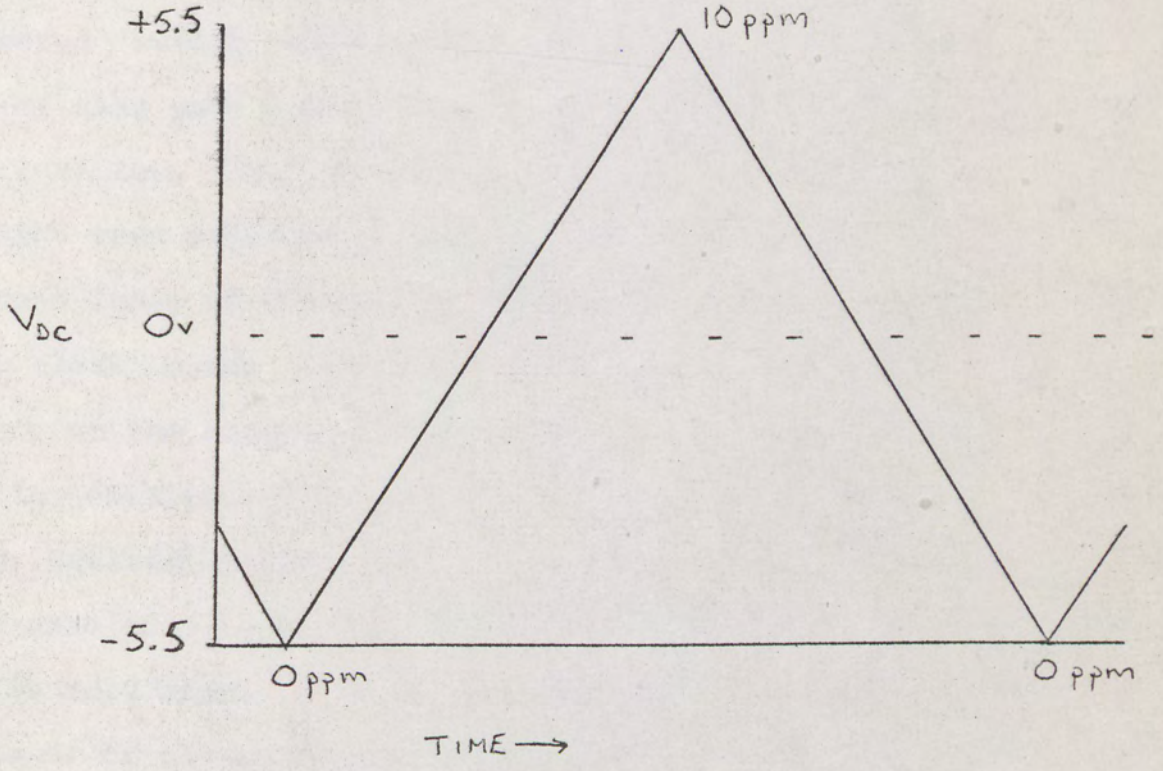
As was discussed in Section I of this report, the P.E. R-24A NMR does not have the ability to continuously scan its spectrum. There were two methods considered for causing the sweep coil to scan continuously; a digitally controlled sawtooth wave generator or one which produced a triangular wave output (see Figure 2-3).

The problem with the sawtooth wave is that a delay in sweep restart would have to be included after the 10 ppm to 0 ppm transition to allow the sweep coil to settle due to its hysteresis. We therefore decided to use the triangular sweep wave along with a necessary computer program alteration to account for the fact that data for a particular point in the spectrum would be out of phase with the data sampled from the previous sweep due to the direction re-

Figure 2-3 (a) Sawtooth wave and, (b) triangular wave.



(a)



(b)

versals at 0 and 10 ppm. The circuit which starts and stops the clock pulse train for the triangular ramp and ADC sampling rate is presented in Figure 2-4. Clock pulses from the system time base are applied to one input of IC2. A 7400 quad NAND gate (IC1) connected in cross-coupled fashion is used to produce an R-S flip-flop. When switch S1 is in position B one input of NAND gate B will be high, therefore the output will have to be high (see Table 1-2). NAND gate A is the complement of B and its output should be low; since both inputs are high pin 3 is indeed low. When S1 is in position A both inputs of NAND gate B will be high, and its output will be low. This circuit comprises the commonly encountered "switch debounce". With S1 in position B the output of NAND gate B will hold the borrow line of IC5 (see Figure 2-5) low, which as will be explained further on, causes the ramp value to be held at its maximum of 5.5V. The second input of IC2 is also connected to pin 11 of IC1 thus no clock pulses are being sent to either the sweep generator or the analog to digital converter. When S1 is placed in position A pin 11 of IC1 goes high; thus the leading, positive going edge of each clock pulse will cause the AND gate to conduct and produce clock pulses as long as pin 10 is held high. Switch S1 is the toggle located on the front panel of the sweep generator module; positions A and B are labeled "release" and "initialize" respectively.

Figure 2-4 Switch debounce.

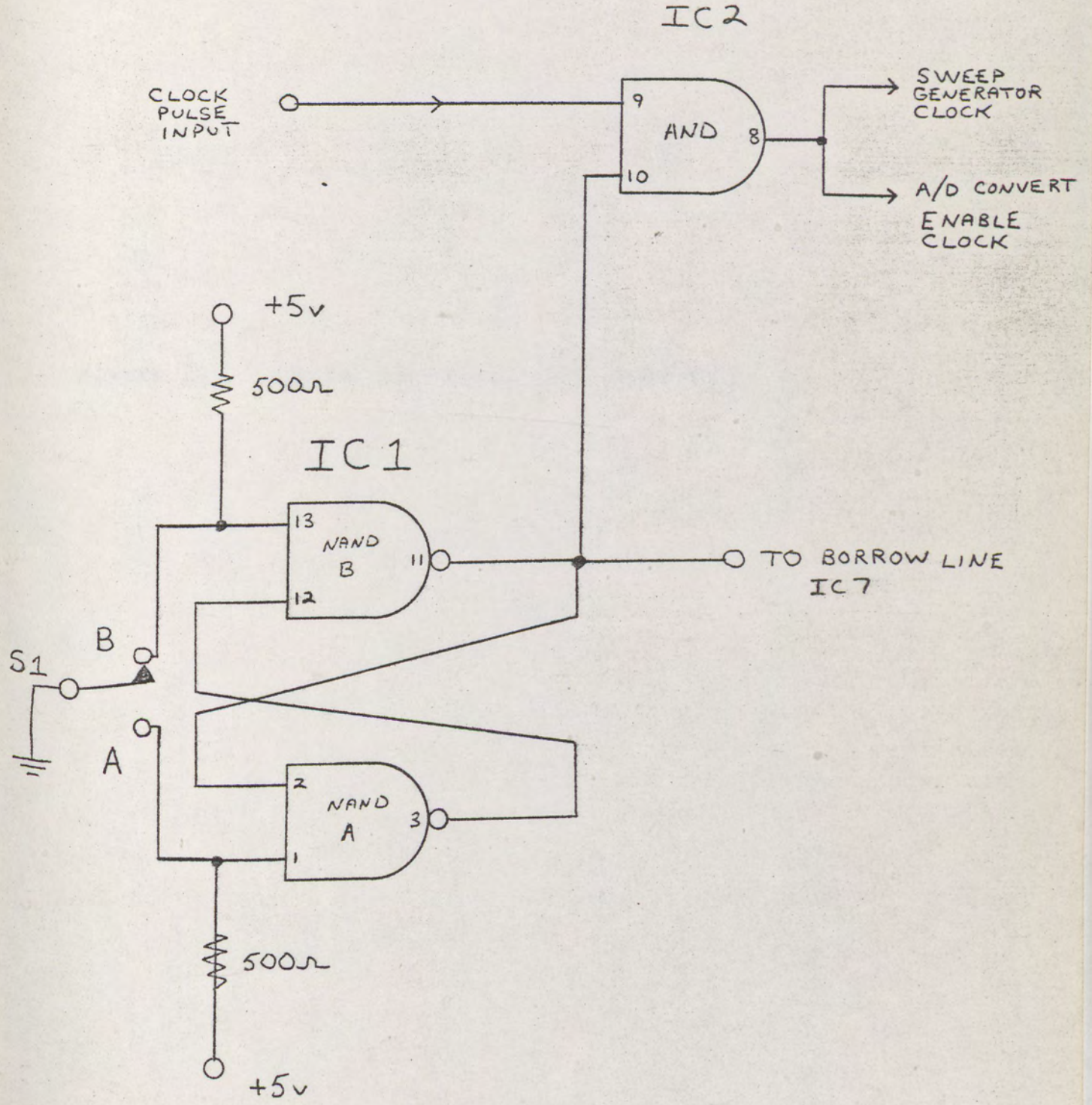
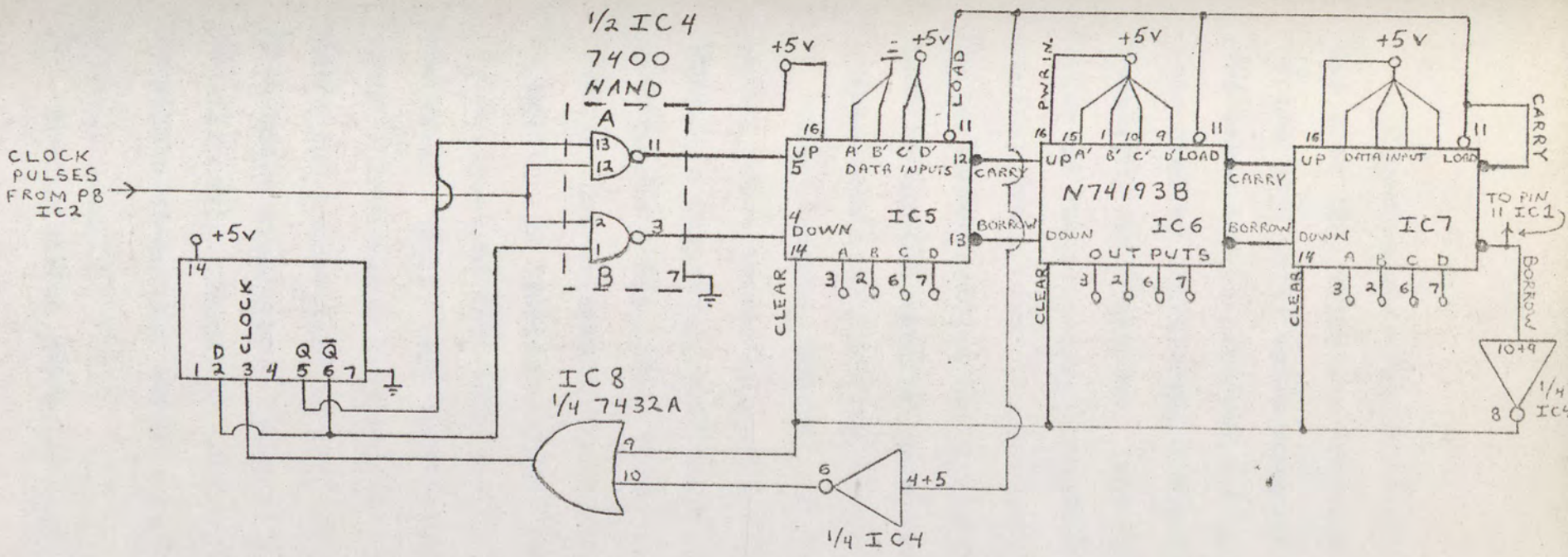
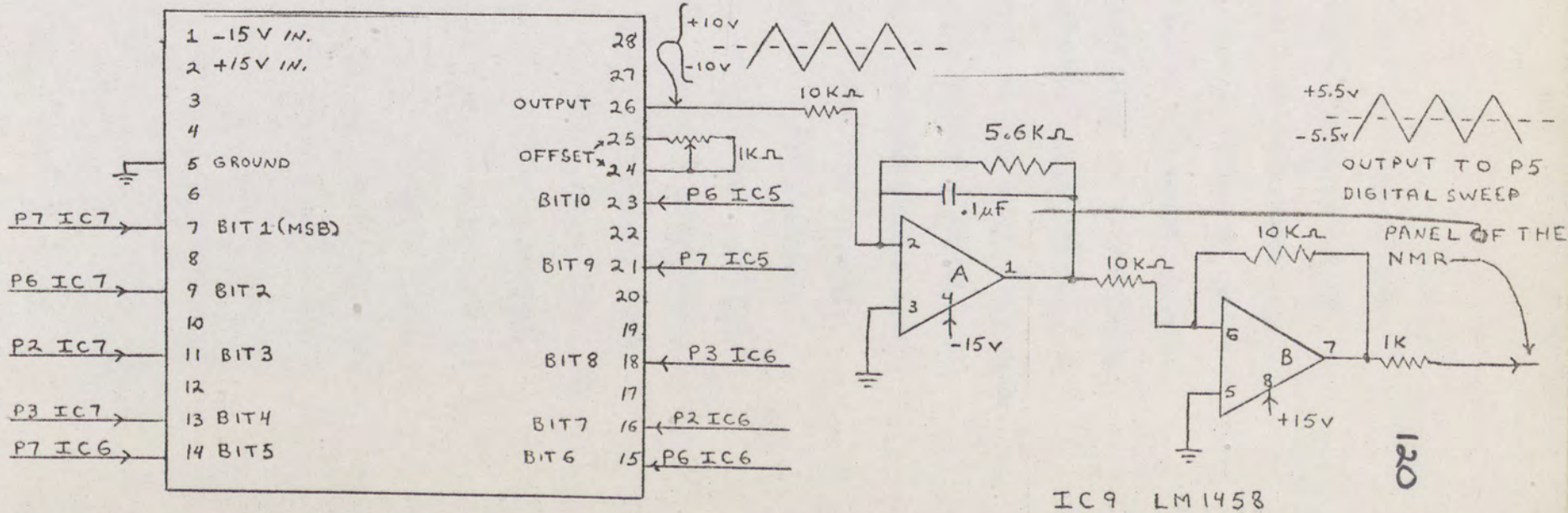

IC2
CLOCK PULSE INPUT
9
AND
8
10
SWEEP GENERATOR CLOCK
A/D CONVERT ENABLE CLOCK
+5v
500Ω
IC1
13
NAND B
11
12
TO BORROW LINE IC7
S1
B
A
2
NAND A
3
1
500Ω
+5v

Figure 2-5 Digital triangular wave generator.





DAC-10Z-3 DIGITAL TO ANALOG CONVERTER

IC9 LM1458
DUAL OP-AMP

Clock pulses from pin 8 of IC2 are coupled to pins 12 and 2 of IC4, which are one-half of the input pairs of two of the NAND gates which comprise the quad 7400 NAND gate. The other inputs of these two gates (pins 13 and 1) are connected to the N7474A, a dual D flip-flop[1] with complementary Q and $\overline{Q}$ outputs. The positive edge of an incoming pulse to the flip-flop's clock input will cause whatever logical state (0 or 1) that is present at the data (D) input to be transferred to the Q output. Since the D input is tied to the $\overline{Q}$ output, Q and $\overline{Q}$ outputs will alternate logic states each time the flip-flop's clock input is pulsed.

The counters, IC5, 6, and 7, produce the changing binary input to the digital to analog converter. As discussed in Chapter I, Section D, (see Counters) the N74193 synchronous 4-bit binary up/down counter has present capability. Let us assume that switch S1 of the switch debounce is set in its "initialization" position (A). The counters are designed so that when a high going pulse is applied to the clear inputs, they will reset to zero independent of the clock. Inverter C (1/4 of IC4) holds the clear inputs high while the borrow line is held to ground. The OR gate IC8 also has a high output which is tied to the clock input of the flip-flop. Thus the outputs Q and $\overline{Q}$ of the N7474 will be stable since they switch on the leading positive edge of

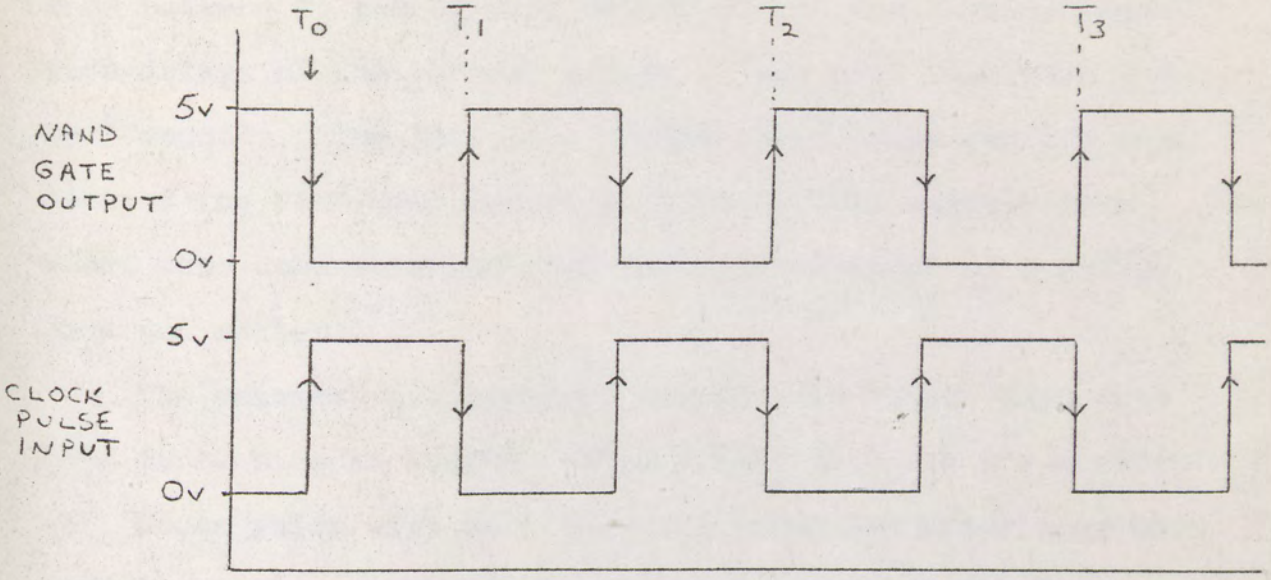
---

1 Specification sheet in Appendix 1.

a pulse to the clock input. When the 26.5 Hz clock pulse train is released (S1 to position B) clock pulses will simultaneously enter pins 12 and 2 of IC4, thus enabling one side each of NAND gates A and B. It is possible for either Q or $\overline{Q}$ to be high at the time that the clock pulses are released. If we assume the ideal case, which is that Q is high, the following will be the sequence of events. Prior to any clock pulses both the up and down inputs of IC5 will be held high; this occurs because both inputs to a NAND gate must be high for the output to be low. The arrival of the first clock pulse will cause the output of NAND gate A to go low (see Figure 2-6). At the fall time of the first clock pulse (rise time of the NAND gate output), T_1, the first change in output state of the counter will occur and Q_A will change from a logic 0 to a 1. The continuation of this count up sequence is illustrated in Figure 2-6.

If $\overline{Q}$ had been at a logic level high initially, the first clock pulse would have caused a negative voltage transition at the down input of IC5. Examination of the timing chart for the N74193 will reveal that with all outputs low, the trailing negative going edge of the pulse entering the down input will cause a borrow to occur (see Figure 1-27). At the leading edge of the negative going borrow pulse the Q and $\overline{Q}$ outputs of the flip-flop will exchange states enabling the UP NAND gate (A) of IC4. This

Figure 2-6 Timing for clock input vs. NAND gate output, and count up sequence.



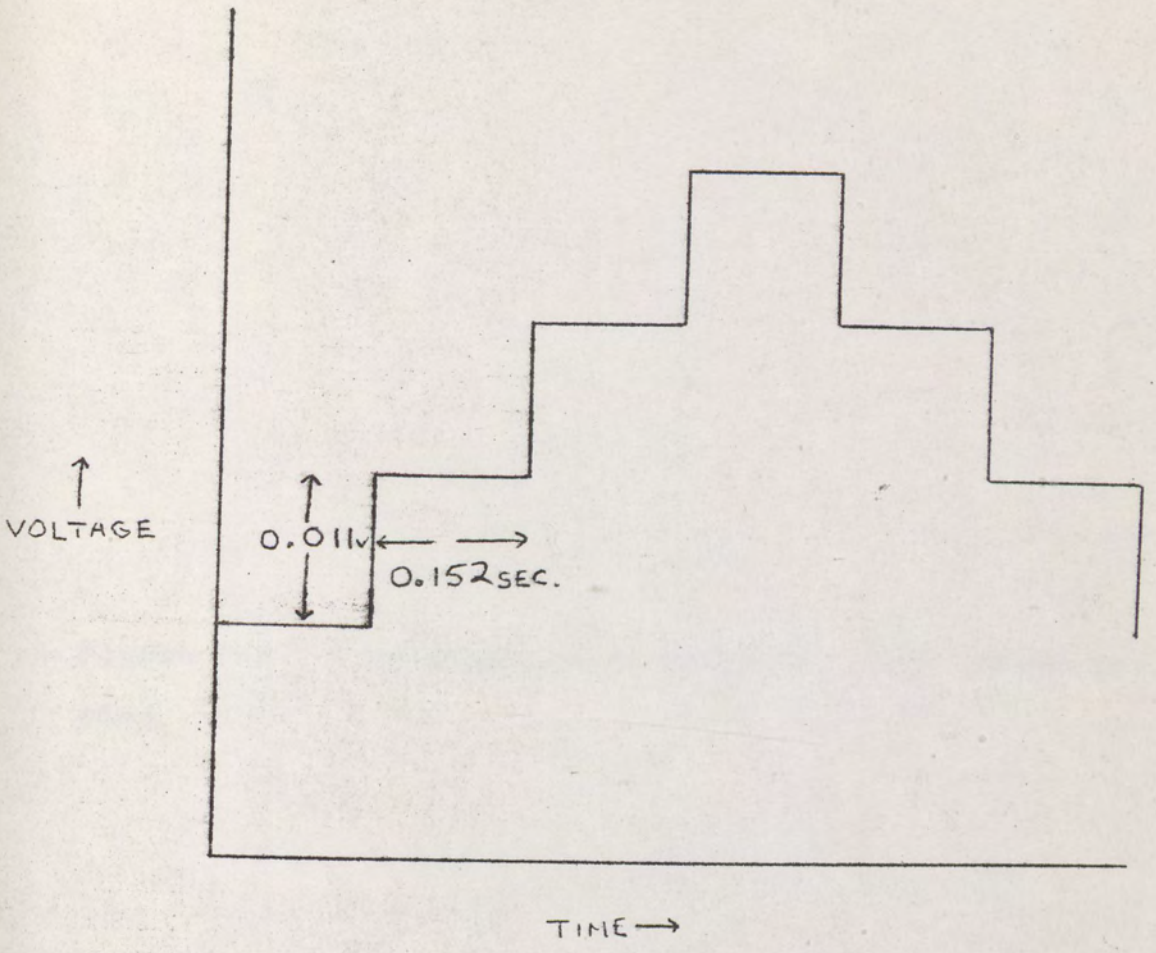
	OUTPUTS				
TIME	Q_A	Q_B	Q_C	Q_D	DECIMAL EQUIVALENT
T_0	0	0	0	0	0
T_1	1	0	0	0	1
T_2	0	1	0	0	2
T_3	1	1	0	0	3

will occur shortly after T_0 (see Figure 2-6) so that the up line of the counter will still be pulsed. The time difference between T_0 and T_0' will depend on the additive propagation delays of the various gates; in our case less than 3 x 10^{-6} seconds. The fall time of the clock pulse and the rise time of the NAND gate output at time T_1 will exactly coincide, thus demonstrating that the initial state of Q and $\overline{Q}$ does not matter.

The counters are cascaded so that the output word from them is 12 bits in length. When all 12 bits are 1's a carry will occur which will pull the load lines low presetting the outputs to the values of the data inputs, A through D on each chip. Simultaneously the direction of count will be changed and a clock pulse entered at the down input of the first counter. Thus the width of the top of the ramp is equivalent to the width of all other ramp steps; Figure 2-7 should aid in the clarification of this point.

The changing output word is continuously monitored by the digital to analog converter. The MSB of the counters is Q_D (pin 7) of the last counter IC7. This is tied to pin 7 (bit 1) of the D/A. The D/A is limited to a 10 bit input word so the LSB of the data is Q_C (pin 6) of IC5. This has important implications in regard to circuit timing. Let us assume that a ramp step has just occurred (see Figure 2-8). The first clock pulse subsequent to the ramp step will force

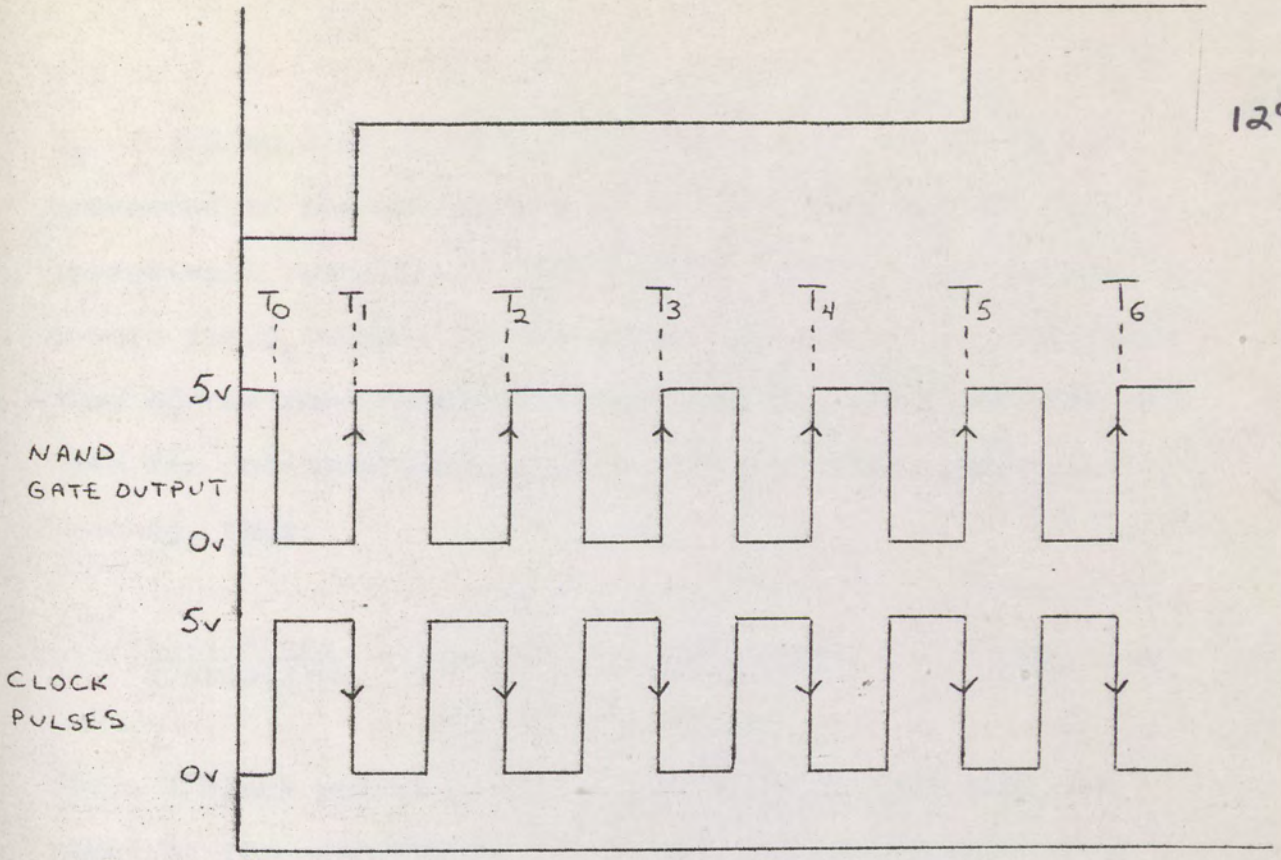
Figure 2-7 Stepwise output of digital to analog converter showing equivalent step widths.



$$\text{STEP HEIGHT} = \frac{\text{TOTAL } \Delta \text{ VOLTAGE OF RAMP}}{\text{NUMBER OF STEPS}} = \frac{11.0\text{v}}{1024} \doteq 0.011\text{v}$$

$$\text{STEP WIDTH} = \frac{1}{\text{STEPS/SEC.}} = \frac{1}{6.56} = 0.152 \text{ SEC.}$$

Figure 2-8 Time relation of number of clock pulses per ramp step.



Bit Pattern

TIME	BITS
T_0	--X11
T_1	--$\bar{X}$00
T_2	--$\bar{X}$01
T_3	--$\bar{X}$10
T_4	--$\bar{X}$11
T_5	--X00
T_6	--X01

X AND $\bar{X}$ ARE COMPLEMENTARY; THEY EQUAL 0 OR 1.

Q_A of IC5 to a high state. But since this output is not connected to the D/A no change in the output of the converter will result. In fact it will take 4 clock pulses before the Q_C output of IC5 changes from 0 to 1. Thus each step of the ramp requires 4 clock pulses. The NMR's sweep rate for one complete spectrum scan is approximately 155 seconds, thus:

$$\frac{1024 \text{ steps}}{x \text{ steps/sec}} = 155 \text{ sec.} \quad x = 6.62 \text{ Hz} \qquad \text{Eqn. 2-4}$$

Since 4 clock pulses are required for each ramp step the required frequency is 4x or approximately 26.5 Hz.

It should be remembered that the 26.5 Hz clock pulse that steps the counters is also used to initiate sampling of the analog output of the NMR by the ADC. Because there are 1024 steps in the sweep range, sampling the NMR's signal 4 times every step would overflow the Altair's 4096 word memory capacity (see Chapter III). To prevent this either another divide by n counter could have been used to reduce the sampling rate, or the program could be altered so that groups of 4 data points are taken into the computer, averaged, and then the average stored. We chose the latter course to prevent this problem.

The output of the D/A is bipolar and varies between +10V and -10V. A 1K ohm offset pot must be attached across

pins 24 and 25 of the D/A so that the output of the D/A (as measured at pin 26) can be set +10.000V $\pm$ 2mV, with a digital input to the D/A of all zeros. This is easily done when the sweep generator is in the initialize state, since all counter outputs are cleared.

The output of the D/A is connected to IC9 (see Figure 2-5), an LM1458 dual operational amplifier. IC9 and its associated circuitry serves to scale down the output of the D/A to the voltage requirements of the NMR's sweep control circuitry. The formula for determining the output voltage (e_o) of an op-amp connected in feedback mode is:

$$e_{in} = - \frac{R_F}{R_{IN}} e_o \qquad \text{Eqn. 2-5}$$

where R_F is the feedback resistance element, R_{IN} is the input resistance and e_{in} the value of the input voltage[47]. For the first half of the LM1458 the following equation holds:

$$e_o = - \frac{5.6K}{10\ K} e_{in} = \pm 5.60v \qquad \text{Eqn. 2-6}$$

The second operational amplifier is used as a unity gain inverter; it also provides additional isolation from the load.

$$e_o = - \frac{10\ K}{10\ K} (e_{in}) = \pm\ 5.60\ v \qquad \text{Eqn. 2-7}$$

The resulting waveform fed through a 1K ohm resistor provides the necessary ramp from -5.5v to +5.5v. The connection to the NMR is through the orange shielded cable which terminates in a jack. Plug P5 from the NMR's digital sweep panel is connected to the jack; when the switch on the sweep generator is put in the release position spectrum scanning will begin.

Specifications for the ramp are based on the 1024 steps that the D/A utilizes. As mentioned previously (see Section B), a clock rate of 6.62 Hz is required to generate a 155 second ramp. Thus,

$$\text{PERIOD} = \frac{1}{6.62\ \text{Hz}} = .151\ \text{seconds} \qquad \text{Eqn. 2-8}$$

is the time width of the ramp step.

The linearity of the ramp is given by the following equation:

$$\frac{\text{ABSOLUTE VOLTAGE VALUE OF RAMP}}{\text{NO. OF STEPS IN RAMP}} = \frac{10.5v}{1024} \doteq 1\%\ \text{OF FULL SCALE}$$

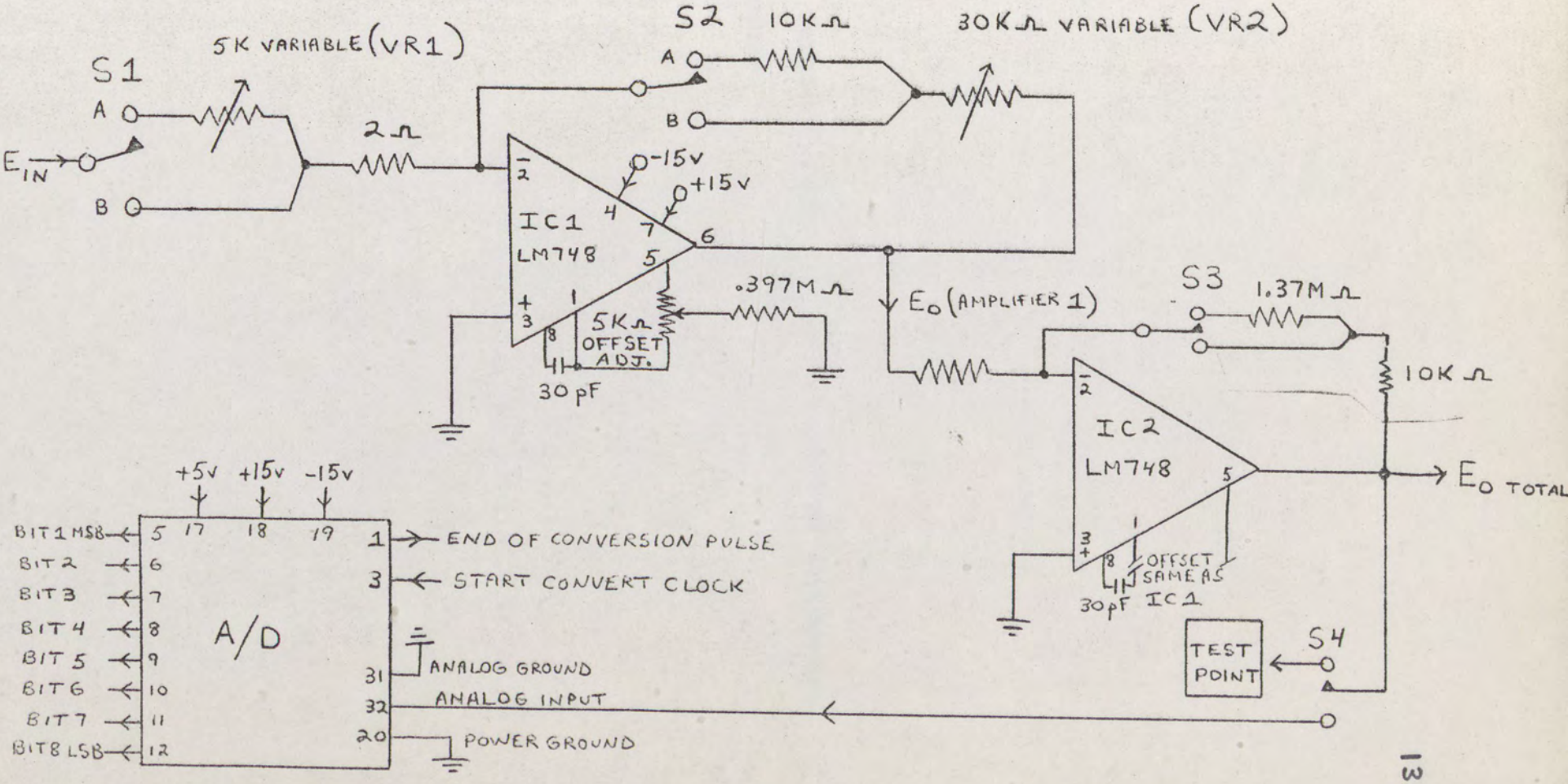
Eqn. 2-9

C. ANALOG AMPLIFIER AND ANALOG TO DIGITAL CONVERTER MODULE

The peak-to-peak noise level from the NMR's "signal output" terminals (back panel of the instrument) is on the order of 10^{-5} volts. The analog input requirements of Datel Systems' model ADC-EH8B analog to digital converter is 0 to +10v in the unipolar application. Thus signal amplitude gain of approximately 10^{6} is required to use the full scale unipolar range of the ADC. This is accomplished by a two stage amplifier utilizing the LM748 high performance operational amplifiers. These linear integrated circuits have offset null capability and excellent thermal stability. Figure 2-9 illustrates the way in which these amplifiers have been connected. Both the feedback and input resistance elements of IC1 can be made variable; in fact the amplifiers are capable of very low gain so that when normal concentration samples are run a digitized record may still be obtained. Various combinations of switch positions and variable resistance settings and their resulting analog gain are shown in Table 2-1. Amplifier IC2 can be set via switch S3 for either unity gain or a gain of 1380 (10K = OHM or 1.3M OHM respectively).

The 5K adjustable trim pot for IC1 allows for the DC offsetting of the analog signal with respect to system

Figure 2-9 Analog amplifier and analog to digital converter circuit.



ANALOG TO DIGITAL
CONVERTER ADC-EH8B1

Table 2-1 Possible gain settings for IC-1 of the analog amplifier module.

SWITCH SETTINGS		RESISTANCE SETTINGS*		MAXIMUM E_{IN}. ASSUMING	GAIN OF AMPLIFIER
S1	S2	VR1	VR2	$10_V = E_{OUT}$.	AT E_{IN} MAX.
2 Ω	30K Ω VAR. PLUS 10K FIXED	—	30K Ω	5×10^{-4} V	2.0×10^4
2 Ω	30K Ω VAR	—	1K Ω	2×10^{-2} V	5×10^2
5K VAR.	30K VAR PLUS 10K FIXED	500 Ω	30K Ω	1.25×10^{-1} V	80
5K VAR.	30K VAR.	500 Ω	30K Ω	1.6×10^{-1} V	60
5K VAR.	30K VAR. PLUS 10K FIXED	5K Ω	30K Ω	1.25 V	8
5K VAR.	30K VAR.	5K Ω	30K Ω	1.6 V	6
5K VAR.	30K VAR.	5K Ω	1K Ω	20 V	0.2

* THE HIGHER RESISTANCE SETTINGS ON BOTH VR1 AND VR2 CORRESPONDS TO ~ A SETTING OF 10 ON THE POTENTIOMETER; LIKEWISE A SETTING OF ~ 1 CORRESPONDS TO THE LOWER RESISTANCES.

ground. The test point located on the front of the amplifier module is activated by switch S4. The output of IC2 is connected only to this test point when S4 is in the appropriate position. Connection of an oscilloscope to this test point will allow for preliminary setting of both the offset and gain of the amplifiers. The gain adjustment is particularly important since not more than 20v peak-to-peak signal should be applied to the analog input of the A/D[1].

It is also important to note that the LM748 op-amp will begin to clip the analog output when the output voltage of the amplifier is taken above 25v. In addition changing the amplifier gain via the adjustable pots will change the offset of the amplifiers, in some cases sufficiently to cause the output of the amplifiers to "lock-up" at their upper or lower output limits (± 25v). When viewed via the oscilloscope at the test point, the output of IC2 may, in such a case, appear as a DC offset of either +25 v or -25 v with no analog signal visible even though it is being applied. In such a case the gain should be reduced until the signal un-locks and then both the offset and gain adjusted sequentially and slowly until proper amplitude and position are obtained. It is suggested that the base of the noise level be set at 0 volts.

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1 See Appendix 1, Analog to Digital Converter Specification Sheet.

When switch S4 is put in the "ADC" position the output of IC2 is applied to the analog input of the converter. A start convert clock pulse must be applied to pin 3 of the converter in order to initiate digitization of the analog signal. As mentioned earlier the clock train which is sent to the sweep generator also triggers digitization. The timing relationship between signal sampling and the ramp steps can be seen in Figure 2-10. Signal sampling and counter outputs both occur at the fall time of the clock pulse and are thus synchronized. Data points are taken in groups of 4 as the diagram indicates. The computer program for data acquisition (see Appendix 2 for complete discussion) takes these data groups, averages them, and stores the binary numerical average in specific and unique memory locations. The end of conversion pulse, which is issued by the A/D when the output word has become valid, is used to inform the computer that valid data can be read.

The output lines of the digital to analog converter (bits 1 to 8, pins 4 to 12 respectively) are connected to the 25 pin cinch mounted on the top of the module. The physical layout of the connector is shown in Figure 2-11. A cable then connects the amplifier/converter module to the parallel input/output board of the computer; the wiring of this cable is discussed in Chapter III.

Figure 2-10 Data acquisition timing; T= time of counter output change and time of signal digitization.

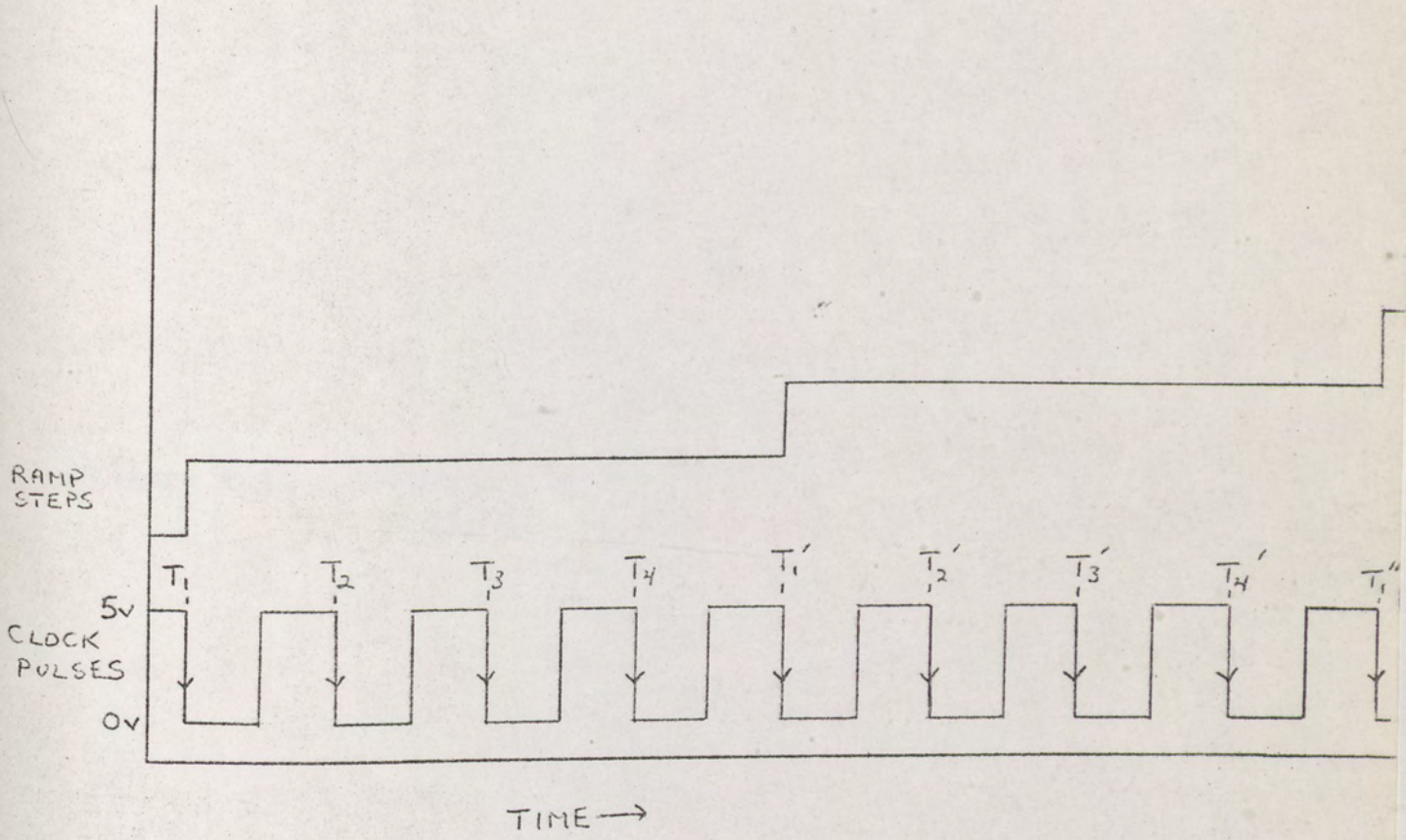
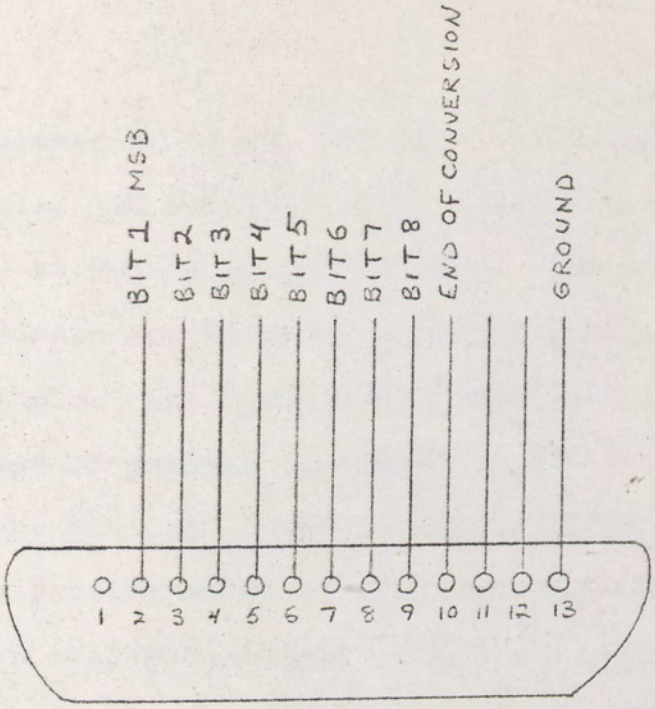

RAMP
STEPS
5v
CLOCK
PULSES
0v
T1
T2
T3
T4
T1'
T2'
T3'
T4'
T1"
TIME ⟶

Figure 2-11 Connector layout for ADC.

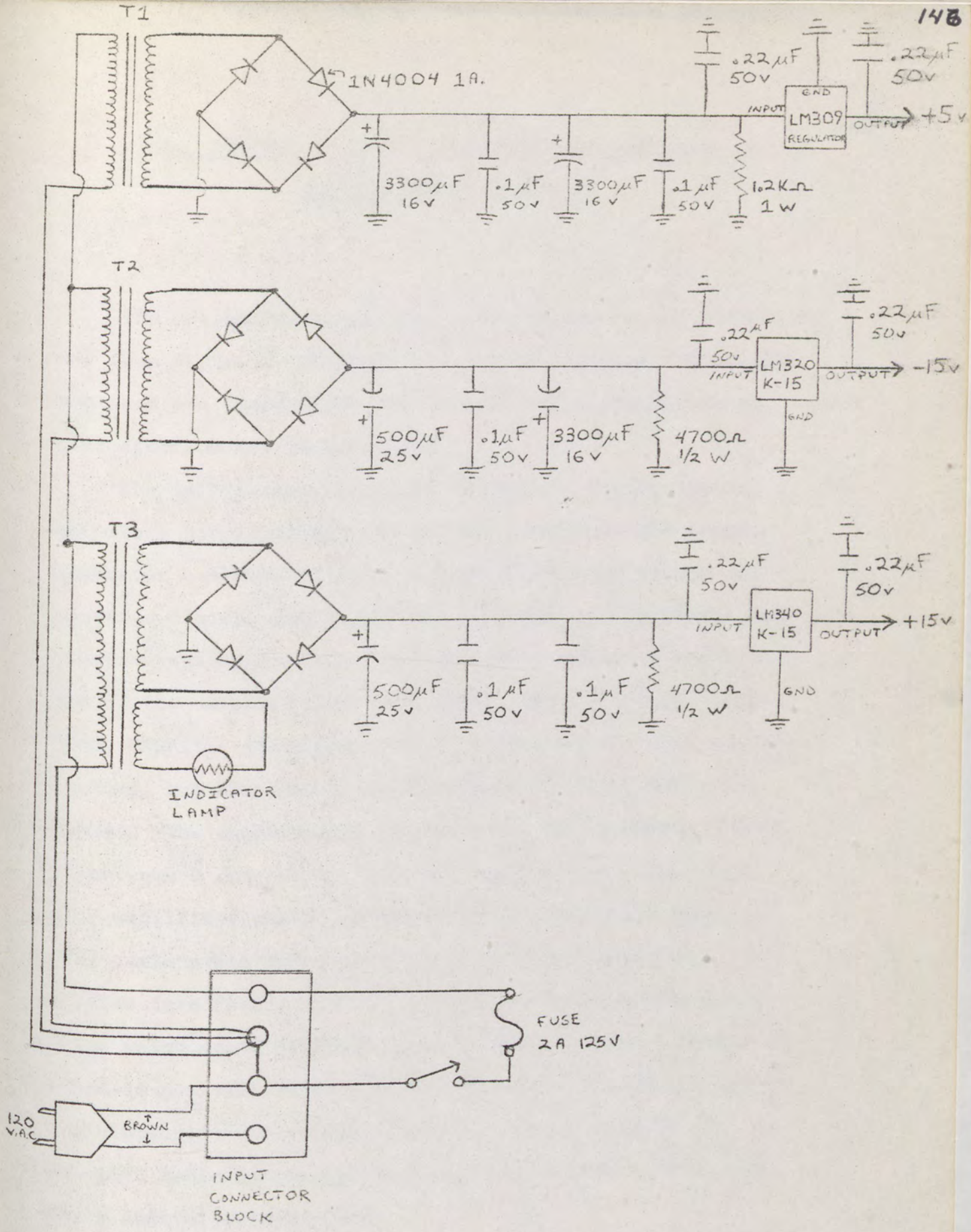

BIT 1 MSB
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
END OF CONVERSION
GROUND
1
2
3
4
5
6
7
8
9
10
11
12
13

D. SYSTEM POWER SUPPLY MODULE

Regulated DC of +5, +15, and -15 volts is supplied by this module. It utilizes three full wave bridge rectifier networks, as Figure 2-12 indicates. The unregulated outputs of the bridges are filtered and decoupled to minimize noise and AC ripple. The resulting DC voltages are then applied to a series of voltage regulators. The 5 volt output is governed by National Semiconductor's LM309K, a complete 5v regulator fabricated on a single silicon chip capable of over 1A of available output current. The regulator is essentially blow-out proof owing to an internal current limiting, thermal shutdown network. The device requires only an input and output capacitor for the rejection of load or line transients (see Appendix 1 for complete specifications).

The +15v and -15v lines are regulated by similar chips: the LM340K-15 and LM320-15 respectively. The DC voltages of all three outputs are constant to within 0.01 v $\pm$ 0.005 v; AC ripple is less than 0.01%. The outputs of the regulators are tied to color coded "banana" jacks; all power input posts on the other modules correspond in color to those on the system power supply.

Figure 2-12 System power supply; T_1 = 6.3vac at 1.2A, T_2 = 16vac at 1.2A, T_3 = 20vac at 1.2A.

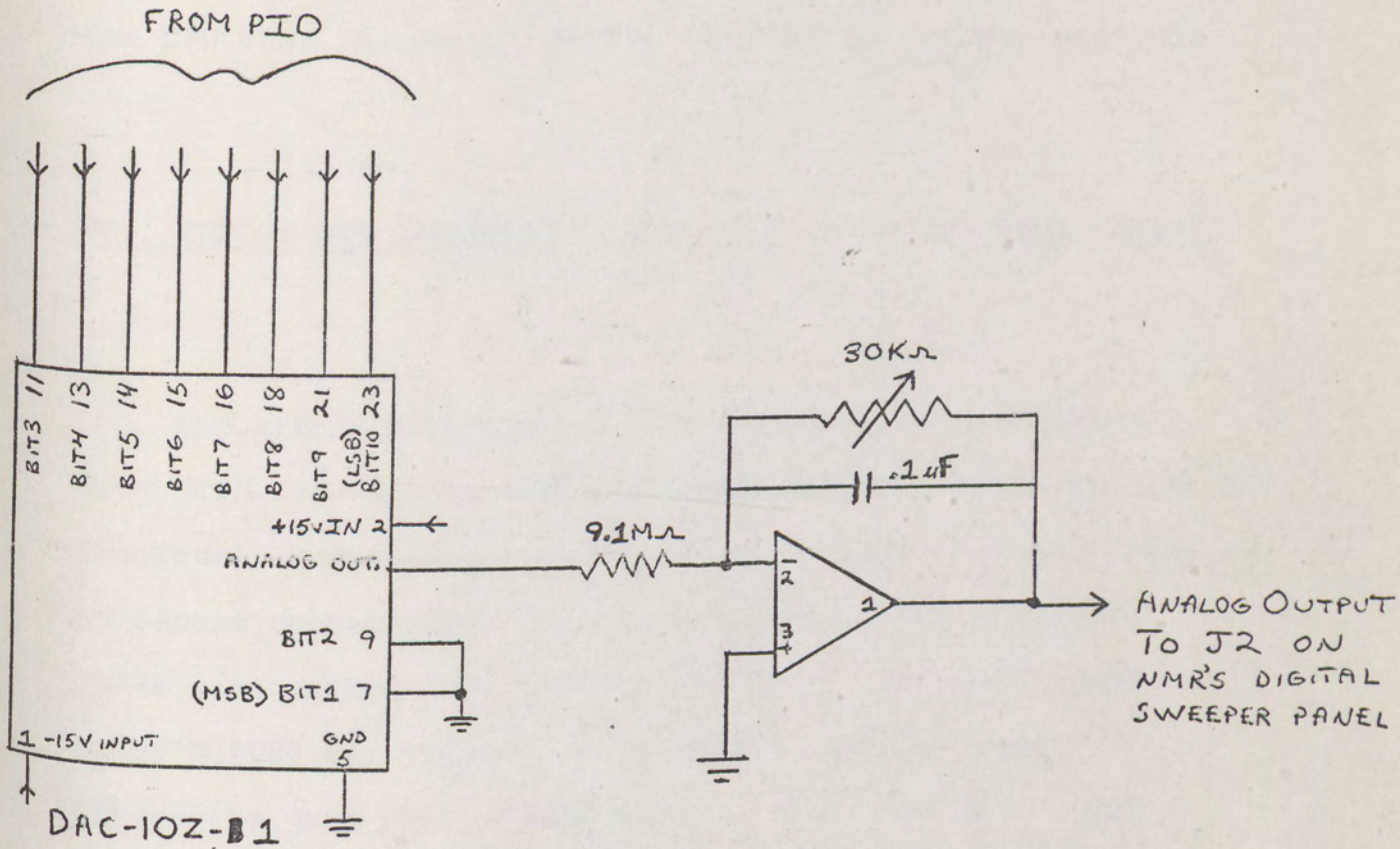

T1
1N4004 1A.
.22μF 50V
.22μF 50V
GND
INPUT
LM309 REGULATOR
OUTPUT
+5V
3300μF 16V
.1μF 50V
3300μF 16V
.1μF 50V
1.2KΩ 1W
T2
.22μF 50V
.22μF 50V
INPUT
LM320 K-15
OUTPUT
-15V
GND
500μF 25V
.1μF 50V
3300μF 16V
4700Ω 1/2 W
T3
.22μF 50V
.22μF 50V
INPUT
LM340 K-15
OUTPUT
+15V
GND
500μF 25V
.1μF 50V
.1μF 50V
4700Ω 1/2 W
INDICATOR LAMP
FUSE 2A 125V
120 V.A.C.
BROWN
INPUT CONNECTOR BLOCK

E. DIGITAL TO ANALOG CONVERTER AND RECORDER INPUT ATTENUATOR MODULE

The D/A converter and the accompanying op-amp attenuator (see Figure 2-13) allow for the de-digitization of the averaged and stored data so that the usual absorbance vs. time spectrum may be obtained.

The information stored in the Altair microprocessor is unipolar; unfortunately the D/A that operates the sweep generator has bipolar input and would respond to the all positive digital output of computer with both positive and negative analog output. Thus we had to order an additional D/A of the unipolar type (DAC-102-1, ANALOG DEVICES, NORWOOD, MASS.). At the time of this writing the part has not arrived, but all associated circuitry has been built and tested. The output of the bipolar D/A is an analog signal of between 0 and -10 v. The NMR recorder contains fixed gain amplifiers which require only a few mV's to produce a full scale swing in the Y direction. The operational amplifier (see Figure 2-3) is an adjustable inverting attenuator which converts the output of the D/A into a signal of suitable positive amplitude (see Equation 2-6 for method of calculation). The output of the op-amp is coupled via shielded cable to the recorder's Y axis input: J2 on the NMR's digital sweeper panel.

Figure 2-13 Digital to analog converter and recorder input attenuator circuit.


FROM PIO
BIT3 11
BIT4 13
BIT5 14
BIT6 15
BIT7 16
BIT8 18
BIT9 21
(LSB) BIT10 23
+15V IN 2
ANALOG OUT
BIT2 9
(MSB) BIT1 7
1 -15V INPUT
GND 5
DAC-10Z-B1
UNIPOLAR DIGITAL
TO ANALOG CONVERTER
9.1MΩ
30KΩ
.1μF
ANALOG OUTPUT
TO J2 ON
NMR'S DIGITAL
SWEEPER PANEL

Synchronization between the field position and the memory location being transferred will be maintained (once again) by the switch debounce circuit which will release pulses to the sweep generator and to the SBO line of the computer simultaneously. Pulsing of the SBO line informs the CPU that the output device is ready to receive new data.

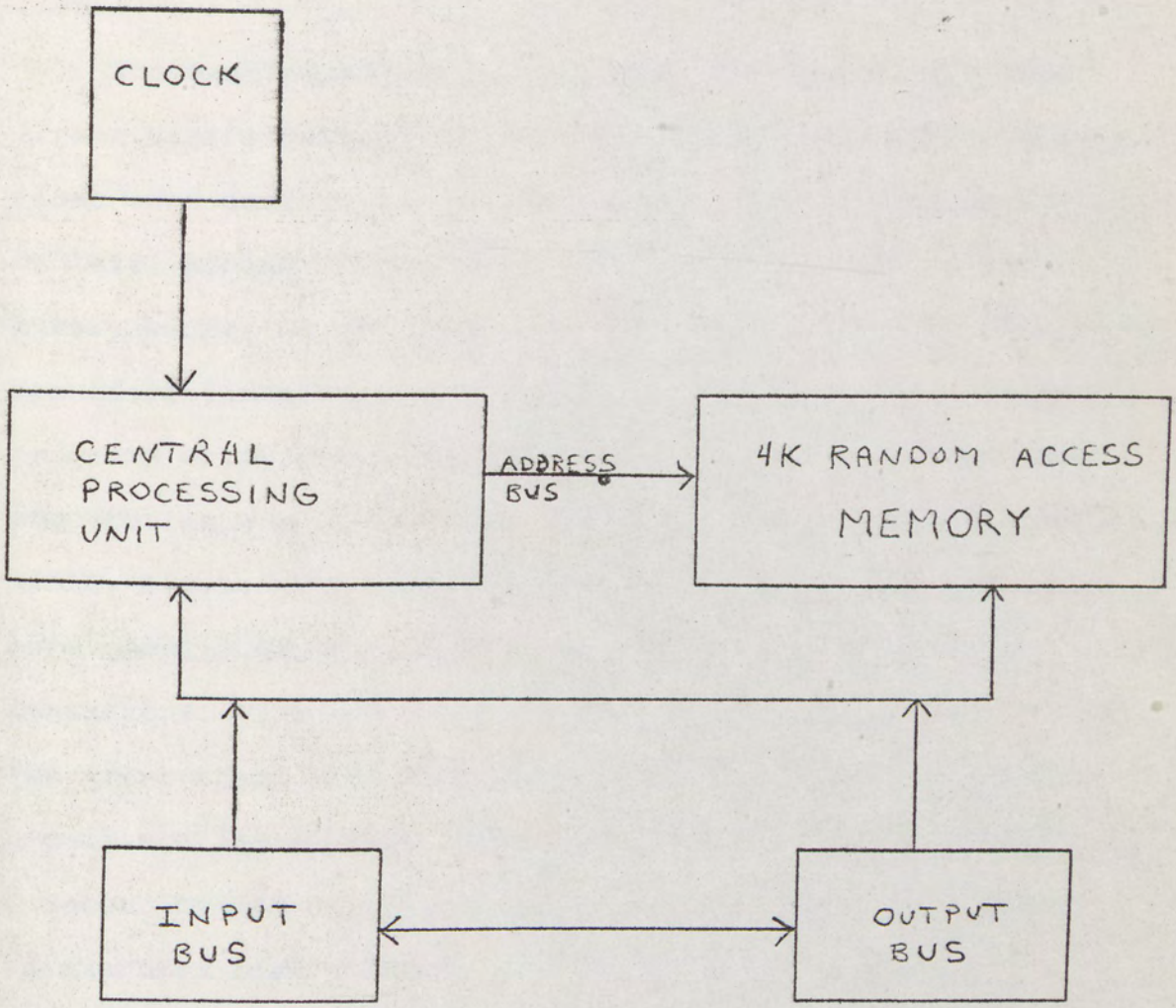
F. THEORY AND OPERATION OF THE ALTAIR 8800 MICROPROCESSOR

The Altair microprocessor was purchased in kit form from MITS Inc. and assembled in approximately 40 hours. As previously mentioned, the 8800 microcomputer is the product of recent technological developments in medium and large scale integration. The entire system is designed around Intel's 8080 microprocessor packet, a complete central processing unit on a single LSI chip. It uses n-channel silicon gate MOS technology; there are 16 separate address lines and an 8 line bidirectional data bus.

The overall organization of the Altair is illustrated in Figure 2-14.

The CPU and Clock: The central processing unit (CPU) includes all of the circuits necessary for the interpretation and execution of program instructions. It performs all

Figure 2-14 Organization of the Altair 8800 computer.


CLOCK
CENTRAL PROCESSING UNIT
ADDRESS BUS
4K RANDOM ACCESS MEMORY
INPUT BUS
OUTPUT BUS

arithmetic and logical operations, stores and retrieves information from memory, controls the input and output of data, and provides for the orderly execution of a program. The program instructions for the Altair are binary coded 8 bit words. These instructions are first stored in memory then retrieved one at a time by the CPU which interprets and executes the command before moving on to the next instruction.

The machine language repertoire for the Altair (see Altair User's Manual) consists of 78 rather simple operations such as rotating the contents of the accumulator right or left, adding the contents of the accumulator to some binary number stored in memory, or the transfer of data to a specified location. Larger computer systems have compiler programs which allow the operator to communicate with the computer in a more familiar language, (e.g., FORTRAN, BASIC, COBAL, etc.). The compiler however merely translates these more complex instructions into a set of far more simple operations. The utility of the digital computer arises from the great speed with which it can perform these operations. A complete instruction cycle is completed in 2 millionths of a second by the Altair; a six instruction addition program is executed approximately 30,000 times in one second[49].

To insure coordinated program execution the Altair 8800 system utilizes a 2.000 MHz crystal controlled TTL oscilla-

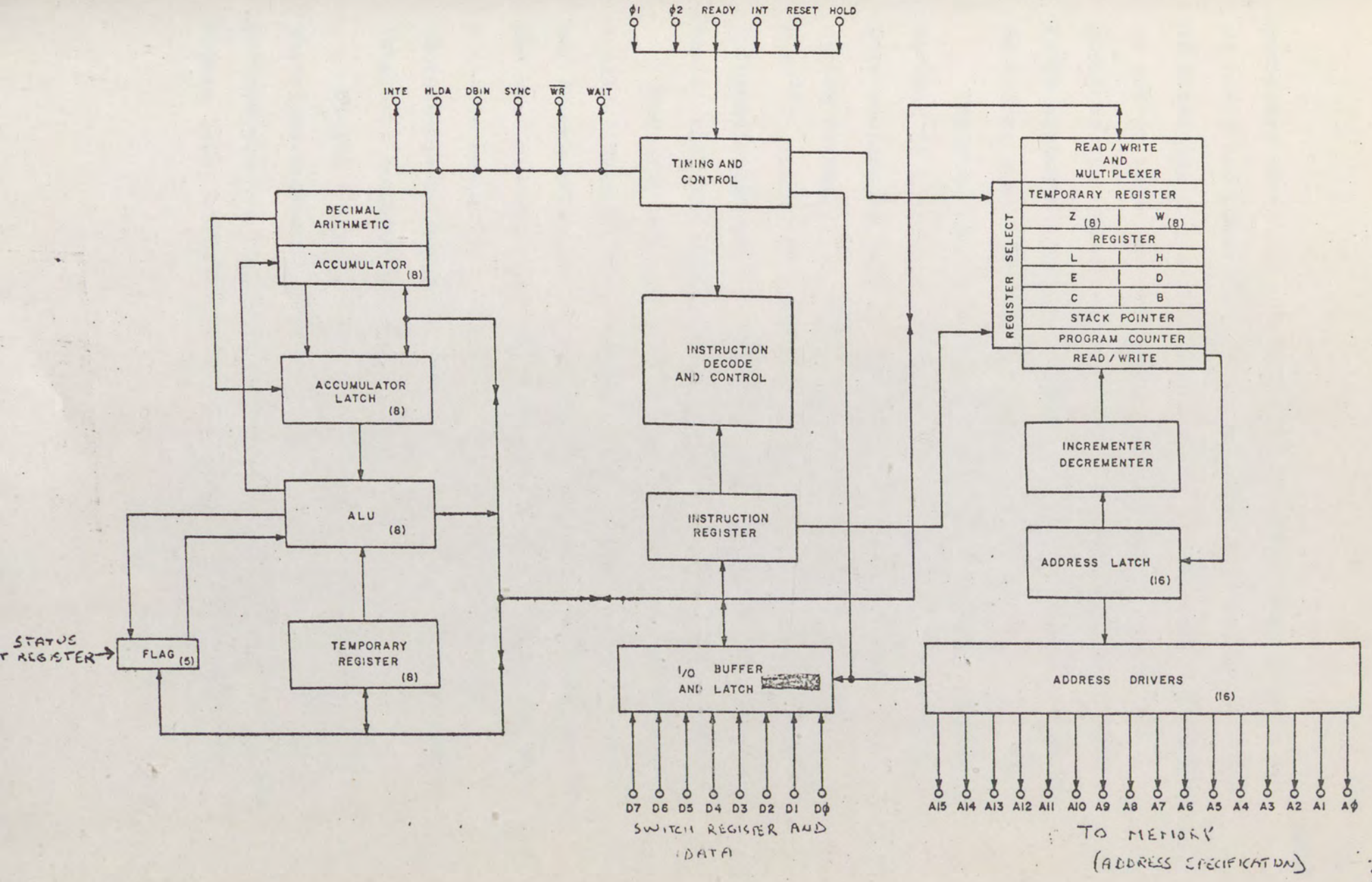
tor to provide timing pulses to the CPU chip (see Figure 2-15). Crystal control is essential because the Intel 8080's maximum operating speed is 2 microseconds and thus a system "speedup" would result in loss of control coordination.

Instructions enter the CPU through the input/output buffer and latch; DØ thrugh D7 constitute the 8 data lines. These commands are temporarily stored in the instruction register (see Figure 2-15) before decoding and execution by the CPU.

Arithmetic operations are done in the arithmetic system of the CPU which comprises the accumulator (which accumulates partial binary number sumes), associated data latches and temporary register[51]. The accumulator (AC) itself is a working register into which the results of many of the computer's arithmetic operations are eventually input. If the CPU may be called the "heart" of the computer, then the AC is the "heart" of the CPU.

There are seven other working registers used in the Altair CPU; the five bit flag register (see Figure 2-15) stores the status of five conditions which may have changed as the result of some data operation. Various program instructions are dependent on the condition of these status bits. The carry bit of the flag register is set to a logical 1 if a carry has occurred out of bit DØ or D7 as the result of manipulation of the accumulator contents. An

Figure 2-15 CPU organization.


φ1
φ2
READY
INT
RESET
HOLD
INTE
HLDA
DBIN
SYNC
WR
WAIT
TIMING AND CONTROL
READ / WRITE AND MULTIPLEXER
TEMPORARY REGISTER
Z (8)
W (8)
REGISTER
L
H
E
D
C
B
STACK POINTER
PROGRAM COUNTER
READ / WRITE
REGISTER SELECT
DECIMAL ARITHMETIC
ACCUMULATOR (8)
ACCUMULATOR LATCH (8)
ALU (8)
INSTRUCTION DECODE AND CONTROL
INSTRUCTION REGISTER
INCREMENTER DECREMENTER
ADDRESS LATCH (16)
STATUS REGISTER
FLAG (5)
TEMPORARY REGISTER (8)
I/O BUFFER AND LATCH
ADDRESS DRIVERS (16)
D7 D6 D5 D4 D3 D2 D1 Dφ
SWITCH REGISTER AND DATA
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 Aφ
TO MEMORY (ADDRESS SPECIFICATION)

auxiliary carry bit can be set to indicate when a carry out of bit 3 has occurred (see DAA instruction, instruction set of Altair). The sign bit of the status bit register is set to indicate the sign of a result. The zero bit monitors the accumulator for results which are zero. The fifth status bit checks whether the sum of 1 bits in the AC is odd or even; this is the parity bit.

The other six working registers are arranged in pairs so that 16 bit operation can be accomplished as when a high core address is used or when data is needed in double precision format to increase information density per data word[52]. These are called "scratch pad" registers because information is written in and read out on a continuous basis; they are available for various program operations.

Normally a program in the Altair will execute sequentially. This is accomplished by the program counter register in the CPU. This register stores the 16 bit address of the next program step and is automatically incremented upon a step's execution. The program register is directly addressable by the JUMP, CALL and RETURN instructions which interrupt sequential program execution[53].

During the execution of subroutines (where the above three instructions are used) the present contents of the program counter is placed in the stack pointer register (see Figure 2-15) while the subroutine is executed. Upon com-

pletion, the RETURN instruction will cause the transfer of the stack pointer contents back to the program counter and main program execution will continue.

More than one piece of information may be stored via the stack; a block of memory may be designated by the LXI instruction and the stack can then be utilized as a stored list of data on a last in, first out basis.

Memory: Program and bulk data storage in the Altair system is done on the 4K random access dynamic (RAM) memory board. 4,096 8 bit words may be stored on each memory board in the dynamic memory cells which consist of a capacitor and associated transistors that sense, maintain or change the charge stored in the dielectric[1]. The Altair's memory is expandable to 65,536 8 bit words.

The CPU controls the access of memory as Figure 2-14 illustrates. The 16 address lines (AØ to A15) connect the CPU to the memory which allows for data transfer from the 216 = 65,536 memory locations. Data moves between the CPU and memory via the 8 bidirectional data lines of the data bus.

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1 In Section II flip-flops were used to illustrate memory applications. Static memory cells do consist of these bistable devices; the Altair does not use them for design reasons which include the dynamic cells, faster access time and lower power dissipation[54].

Operation of the Altair Microprocessor: Communication with the Altair is done through the 25 toggle switches and 36 indicator LED's on the display control panel. Through these the operator may examine and modify any location in memory.

The best way to learn how to use the Altair is to input and run a program. One begins by putting the on-off switch into the on position (when turned off memory is wiped out) which supplies all boards with the necessary DC supply voltages. Since the computer will come up in a random state the stop/run switch must be held in the stop position, while the reset/clear (CLR) switch is held to reset. Reset sets the program counter to the first memory location, 0 000 000 000 000 000.

Since the 4K memory board has a protect feature which when activated prevents the alteration of memory locations, before one can program the protect/unprotect switch must be thrown. One then places the first 8 bit byte into the computer by putting the sense switches into the appropriate 1 or 0 state, and pressing the deposit/deposit next switch in the deposit direction*. Subsequent words are entered in a similar manner with the exception that the deposit next

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* An excellent reference on microprocessor programming (a subject too extensive to be covered in this report) can be found in Reference #23.

switch is used; this places the instructions sequentially in memory.

To check to see if the program has been loaded correctly, one presses reset and then the examine - next switch to view the contents of memory. If an instruction has been entered incorrectly merely stop at the incorrect statement (or load the address of the incorrect statement into the sense switches and press examine) and reload the sense switches with the correct command and press deposit.

A program does not have to begin at memory location 0; in fact subroutines and specified data blocks may have to be rather "high" in core memory. By loading the sense switches with the desired starting address and then pressing examine this is easily accomplished.

The single step switch on the display/control panel allows the operator to run a program one step at a time; this is important because the operator can check the status indicators to see if the computer is in the correct cycle and to check for proper program execution. If this switch is activated the stop switch must be thrown when the examination has been completed for the computer is essentially in the run mode. When the run switch is thrown the computer will execute the program at the normal rate.

Various computer operations may be monitored via the status LED's; Table 2-2 shows the condition which is indicated by a glowing status LED[55].

Table 2-2 Significance of status LED states.

LED	OPERATION
MEMR	Indicates that the data bus will be used for memory read data.
INP	The address device has been loaded with the address of an input device. When the processor issues an input mode signal the input data will be placed on the data bus.
M1	Processor is fetching the first byte of a command.
OUT	The address bus contains an output device's address. Upon processor issued ready signal data will be placed on the data bus.
HLTA	A HALT has been issued and executed.
STACK	The address bus has been loaded with the push-down stack address.
WO	A WRITE (w) or an OUTPUT (O) is the current machine operation.
INT	An external device has issued an interrupt to the computer for data input, output or status specification; the glowing LED indicates the condition is acknowledged.
INTE	The CPU has been instructed to enable interrupts; when an interrupt is received the computer will now be able to act accordingly.

P. 163 missing due to typographical error

Input and Output Structure: Knowledge of the computer's input/output structure is the key to understanding the microprocessor's role in the chemical laboratory. Initially, the sense switches are the primary method of communication; the essential advantage of the digital computer however is neglected by using only these. With a response time on the order of millionths of a second the computer spends most of its time waiting for the input of data. Various input/output devices, such as the Teletype and high speed paper tape punch, improve on this crude method of communication.

The Teletype (TTY) is representative of a class of serially oriented input/output devices; it is also the most commonly used laboratory interface for computer/operator communication. Digital signal levels are transmitted from the TTY along a pair of twisted wires to the computer's serial I/O board. These signals are generated by pressing one of the over 100 different alphanumeric and symbolic characters on the TTY keyboard. A keyboard entry causes unique 8 bit code (designated by the American Standard Code for Information Interchange, ASCII) to be placed simultaneously on a series of contacts located radially about a circle which is swept by a commutator arm. The serial bit string mentioned above is the result. Similarly data in ASCII code is accepted by the TTY and converted to a printed character.

Data entry via the TTY/serial input-output interface is fast compared to the toggle-in procedure outlined earlier; it is still much slower however, than the computer's normal operating speed. A standard TTY has an I/O rate of only 110 bits per second (i.e., 110 baud); therefore control lines are necessary which will inform the computer when the TTY has sent or is ready to receive new data. These control channels are monitored for the Altair by the serial interface board.

The Serial Input/Output Board: Structure and Operation: The 88-SIO C board is a standard TTY level interface board which was purchased in kit form from MITS Inc. (as was the entire Altair microprocessor system). The control center of this interface is the Universal Asynchronous Receiver-Transmitter (UART) chip; this LSI device provides serial to parallel and parallel to serial conversion along with flag signals, which indicate the readiness of the chip to transmit or receive new data[56].

For the computer to accept data from the TTY, an input instruction must be executed. This command consists of two bytes, the first being the input instruction the second being the address of the input/output board:

Input Information - BYTE 1 - 11 011 011 = 333_8

Specified Address - BYTE 2 - XX XXX XXO = XXX_8 where XXX is 0 to 376_8, even numbers only.

As is indicated the address of the I/O device is selectable, the only stipulations being that it be an even number between 0 and 376_8. We have chosen 050_8 as the address of the serial I/O board, and henceforth this number will represent this board's address. It should be noted that by choosing 050_8 as the SIO board address, 051_8 is automatically designated as the data channel and 050_8 as the status channel[57]. The distinction between the status/control channel and the data channel will be clarified in the following discussion.

Execution of the input command along with the status/control channel address, 050_8, will cause the SIO's control channel to be enabled. This directs the UART to place an 8 bit status word onto the data lines which is then fed into the CPU's accumulator. The 8 bits of this word are defined in Table 2-3[58].

Table 2-3 Control Word Definition

Data Bit	Logic Low	Logic High
D7	Output Device Ready Transmitter Buffer Empty	Not Ready
D6	Not Used	Not Used
D5	Not Used	Not Used
D4		Data Overflow
D3		Framming Error (no valid stop bit)
D2		Parity Error
D1	Not Used	Not Used
DØ	Input Device Ready Data Available to Input	Not Ready

The CPU must now inspect this word to see if data is ready to be accepted; Table 2-4 illustrates this procedure. If bit DØ equals 0 then a new character has been received from the TTY; if DØ equals 1 then the data is not ready and the computer must enter a wait cycle until DØ does equal 0. The value of bit DØ is determined by rotating the contents of the AC to the right one bit (instruction #2, Table 2-4). A carry out of bit DØ will be recorded by the flag register, the status of which is monitored by the jump-if-carry instruction (instruction #3, Table 2-4). If no valid data is

present (bit DØ = 1) then the computer will jump back to the address specified by the JC command.

If DØ equals 0 then processing will continue at the next sequential program location, in this case an input instruction. This time the address of the data channel is used which causes the UART to place the parallel version of the received word onto the data bus and thus into the accumulator. Once in the AC normal data manipulation by the computer may begin.

An output routine would be quite similar to the above, except (as Table 2-3 indicates) the condition of bit D7 of the status/control word determines the readiness of the TTY to accept a new character.

Putting an input and an output routine together generates an "echo" program which causes a character that is typed on the TTY keyboard to be echoed by the computer back to the TTY to be printed; this program is shown in Table 2-5.

We have succeeded thus far in entering data via the TTY keyboard into the CPU of the Altair. The information however is in ASCII code form and therefore must be converted to binary before the computer can perform arithmetic manipulation with it. Conversely the computer must translate all data to be transferred to the TTY into ASCII code before it can be transmitted. Programming manipulations such as these

Table 2-4 Typical input routine for serial I/O board.

BYTE #	INSTRUCTION # XXX_8	INSTRUCTION	OPERATION
1	000	333 IN	Input the status
2	001	050	channel
1	002	017 RRC	Test status of SIO board (is DØ=0?) by rotating AC right
1	003	332 JC	Jump to instruction
2	004	000	# 000 000_8 if a
3	005	000	carry occurred.
1	006	333 IN	Input the contents
2	007	051	of the data channel
1	010_8	062 STA	Store the character
2	011	045	in a memory location
3	012	000	(000 045_8)
1	013	303 JMP	Jump back to beginning
2	014	000	of program and wait
3	015	000	for new character entry

Table 2-5 Echo program.

BYTE #	INSTRUCTION # XXX_8	INSTRUCTION	OPERATION
1	000	333 IN	Input contents of the
2	001	050	status channel
1	002	017 RRC	Rotate AC right
1	003	332 JC	Jump if DØ=1 back
2	004	000	to instruction 000 000.
3	005	000	
1	006	333 IN	Input the contents of
2	007	051	the data channel
1	010	062 STA	Store the character in
2	011	045	memory location 000 045_8.
1	013	333 IN	Input the contents
2	014	000	of the status channel
1	015	007 RLC	Rotate AC left
1	016	332 JC	Jump, if D7=1, back to
2	017	013	instruction 013 and loop until
3	020	000	the VART's transmitter is ready.
1	021	072 LDA	Load the AC with the
2	022	045	data in memory location
3	023	000	000 045_8
1	024	323 OUT	Output contents of AC to the
2	025	051	SIO via the data channel
1	026	303 JMP	Jump back to beginning of
2	027	000	program and wait for a
3	030	000	new character.

are beyond the scope of this report, but are described in a large number of sources[59].

The Parallel Input/Output Board: Binary coded data is entered into, and retrieved from, the Altair via the parallel input/output board[60]. This circuit card is designed for interfacing to 8-bit parallel input/output devices such as the D/A and A/D converters in our application. An input and output 8-bit data latch act as buffers between the microprocessor and the external devices.

As in the case of the serial I/O board, the parallel I/O card has 2 effective addresses which have been selected by hard-wire jumpers on the board. Address 060_8 corresponds to the control channel which is used to test the status of the external device; address 061_8 is the data channel of the card.

During operation of the interface system the SBI line of the input data latch will go pulse whenever valid data is present at the outputs of the A/D converter. Pulsing SBI informs the CPU that the external device is ready to send data. A similar line labeled SBO is used for the purpose of informing the CPU that the external device is ready to receive data.

When an "IN" instruction followed by the even address of the board is encountered in the program, the status bit lines DIØ and DI1 of the input buffer are loaded with the

external device's status. If the device is ready to transmit DI1 will go high; if ready to receive DIØ will go high.

To input data an "IN" instruction followed by the address of the data channel (061_8) is used. Analogously the output of data is achieved via an "OUT" instruction followed by the data channel address. A typical input/output routine is illustrated in Table .

All connections to the parallel I/O board are through a 25 pin cinch connector; Figure 2-16 contains a wiring diagram.

G. THE PROGRAMS

Several programs have been written for the Altair 8800 which accord the user a variety of control and processing options*. The first of these programs is a paper tape loader which must be toggled into the computer by hand through the Altair's switch register. Once in computer memory the program allows for the transfer of information on binary coded paper tape from the Teletype to the computer.

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* These programs were written by Arthur Fritzen of the Computer Science Department at Union College. A complete listing of the programs may be found in Appendix 2.

Table 2-6 Example of (a) an input, and, (b), an output routine for the MITS PIO board.

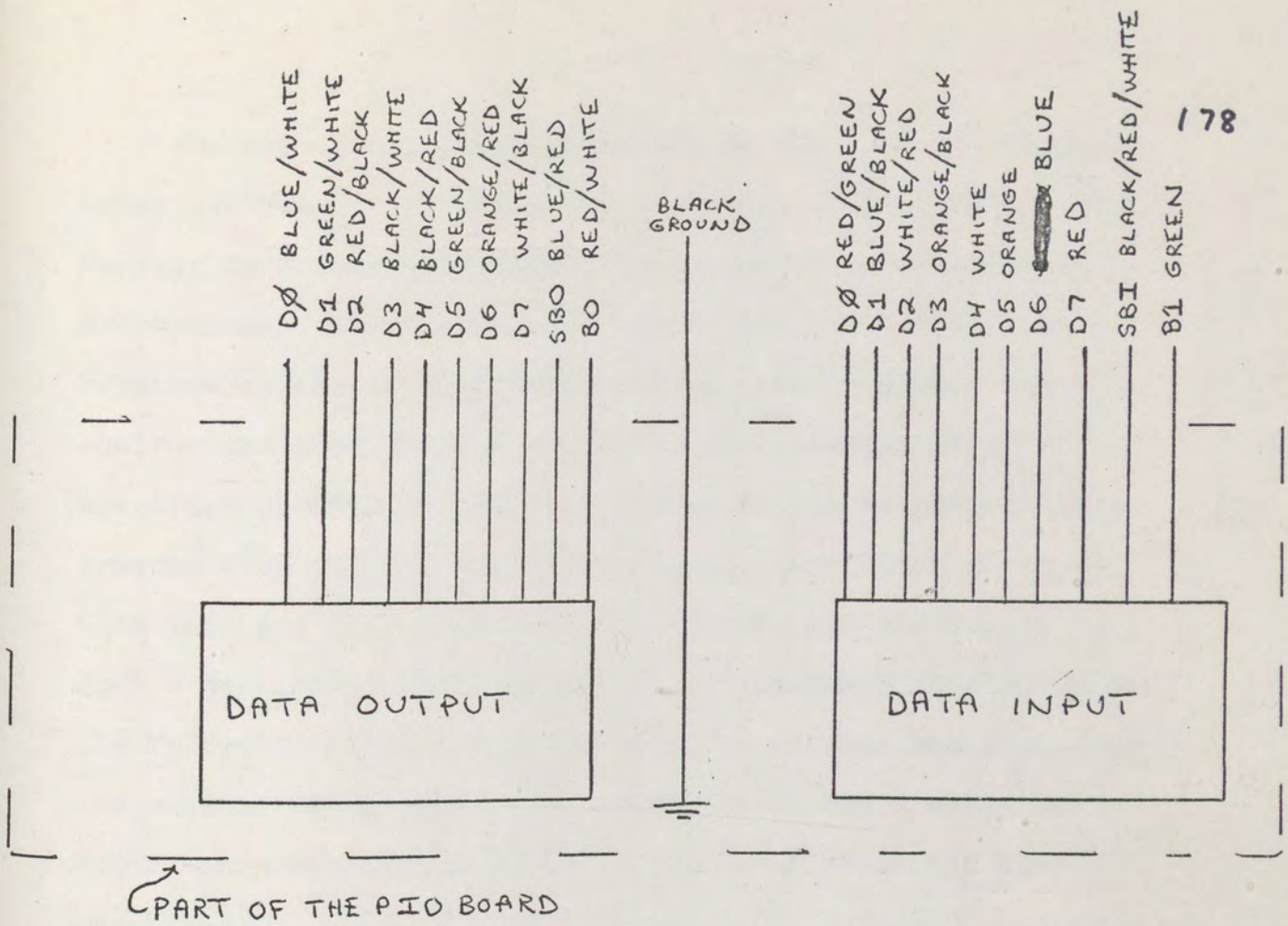
BYTE #	INSTRUCTION #	INSTRUCTION CODE	OPERATION
1	000	333 IN	Input the
2	001	060	status channel
1	002	017 RRC	Rotate accumulator right
1	003	017 RRC	again
1	004	322 JNC	Jump to 000 if bit
2	005	000	D1=0
3	006	000	
1	007	333 IN	Input the
2	010	061	data channel
1	011	303 JMP	Jump to start
2	012	000	
3	013	000	

(a)

1	000	333 IN	Input the status
2	1	060	channel
	2	017 RRC	Rotate accumulator right
	3	322 JNC	Jump to 000 if no
	4	000	carry occurs:
	5	000	DØ = 0
	6	323 OUT	Output data
	7	061	to data channel
	8	303 JMP	Jump to start
	9	000	
	10	000	

(b)

Figure 2-16 Wiring diagram for the Parallel I/O board's data and control lines.



PIO

25 Pin Connector and Cable

B1	11	GREEN
SBI	10	BLACK/RED/WHITE
D7	2	RED
D6	3	BLUE
D5	4	ORANGE
D4	5	WHITE
D3	6	ORANGE/BLACK
D2	7	WHITE/RED
D1	8	BLUE/BLACK
D0	9	RED/GREEN
BO	14	RED/WHITE
SBO	15	BLUE/RED
D7	16	WHITE/BLACK
D6	17	ORANGE/RED
D5	18	GREEN/BLACK
D4	19	BLACK/RED
D3	20	BLACK/WHITE
D2	21	RED/BLACK
D1	22	GREEN/WHITE
D0	23	BLUE/WHITE

The system monitor program may be fed into the computer after the paper tape loader has been placed in memory. The monitor is a complex program consisting of five distinct subroutines. The monitor allows for the writing of new programs at the Teletype keyboard in octal coding. The monitor can also be used to output the contents of any specified section of computer memory to the Teletype. This program also enables the user to load information on paper tape into any specified block of memory, and conversely to dump a designated block of memory to the paper tape punch on the Teletype. A "go" instruction calls another subroutine of the monitor which causes the execution of any program in memory once the starting address of the program has been specified.

The data acquisition program may be loaded once the monitor is in memory. The acquisition program continuously checks the state of the input device, in our case the ADC. When the end of conversion line on the ADC goes low signifying that the output word of the converter is now valid, the SBI line on the Altair's PIO will also go from a logic level 1 to a logic 0. This informs the computer that valid data is present in the PIO's input data latch. As Figure 2-10 indicates there will be four data words per ramp step. The program takes data in groups of four words, averages them together and stores the result in double precision in one of the 1024 assigned memory locations. The problem of the reversal of scan (see Figure 2-3) is accounted for in

the program by loading data in reverse order on alternate ramps. Synchronization is maintained by the counting pulses which simultaneously cause the D/A to step and the computer to access valid data; the program keeps track of the number of clock pulses and the present memory location. After the perscribed number of ramps have occurred, the program divides the contents of each of the 1024 memory locations by the number of ramps, and then stores the result in these same locations. The contents of the table may be transferred in binary code to paper tape, or in a special octal format to the Teletype.

The output program operates in an analogous manner to the acquisition routine, clock pulses to the SBO line of the PIO inform the CPU of the Altair that data may be transferred to the output device. The program causes the contents of each memory location to be dumped four times to the recorder. This is necessitated by the fact that a ramp step requires four clock pulses. Thus for each step in the X direction the recorder will receive the contents of the memory location which corresponds to that spectral position four times.

Chapter III contains a complete discussion of the responses from the computer/interface system that should be expected as well as the commands and procedures that must be followed to make the above mentioned programs operate.

CHAPTER III

SYSTEM UTILIZATION AND FUTURE APPLICATIONS

A. SYSTEM OPERATION

The totally modular design of the computer/interface system makes possible the application of the system to a variety of chemical instrumentation problems. The major thrust of the project up until the completion of this report has been on signal time averaging of NMR spectra, thus this will be the first application to be discussed; applications to gas chromatography will be covered later in this chapter.

The System Monitor: The system monitor program is central to all applications of the computer*. After the paper tape loader program has been entered in computer memory via the front panel switch register, the monitor which is on binary coded paper tape may be loaded into the paper tape reader on the Teletype. The first word of information on the paper tape must be placed over the index holes of the paper tape unit. After careful alignment the

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* See Appendix 2 for listing of all programs.

plastic clasp may be closed over the tape to hold it. At this point the run button on the Altair should be pressed. With the Teletype in the LINE position the start switch on the paper tape unit should be thrown. The paper tape of the monitor will thus be loaded sequentially into memory beginning in location 100_8.

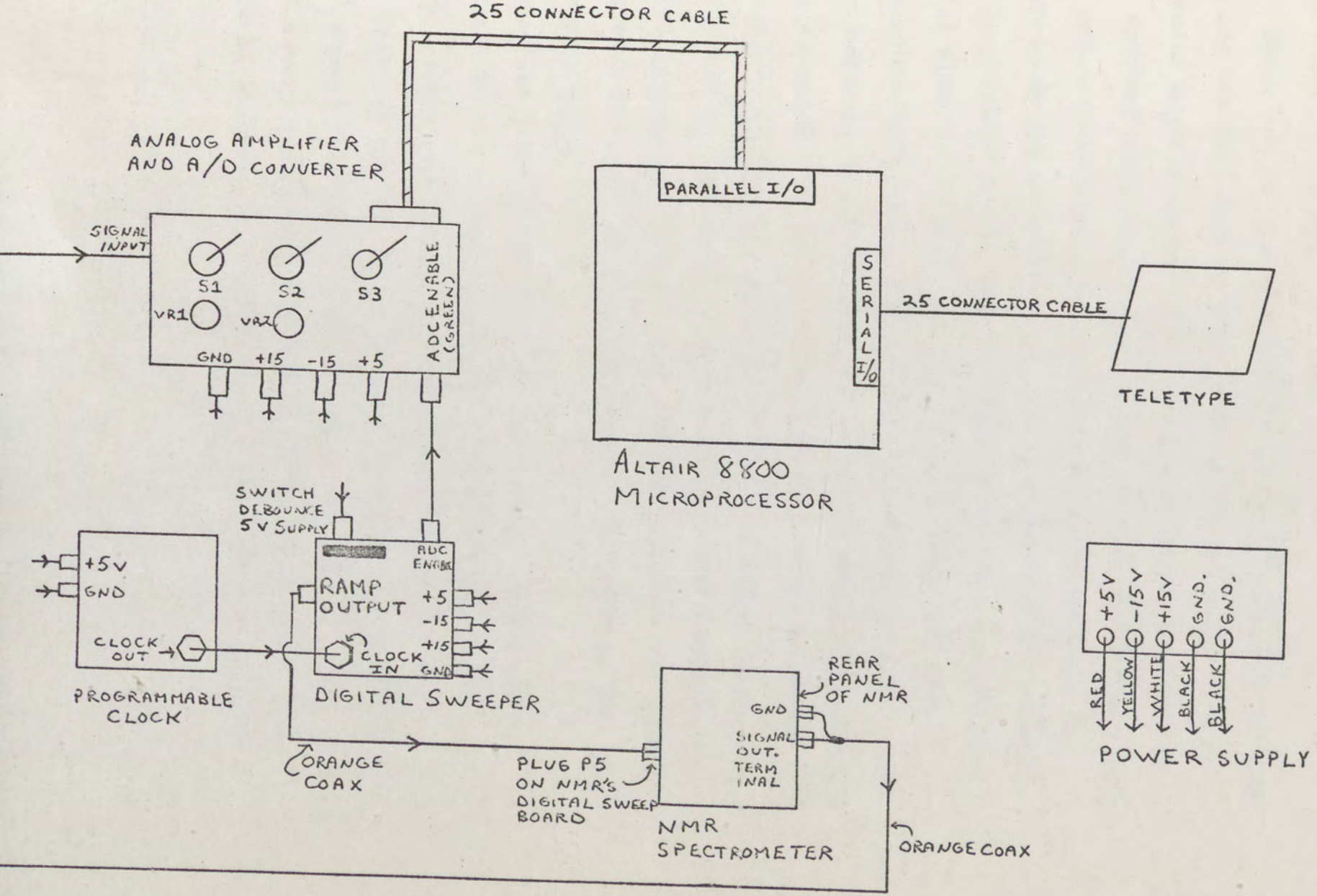
After the program has been read in, location 100_8 should be examined to see if the first piece of binary data on the paper tape has entered this location. To do this press stop, load 1 000 000 onto the sense switches and press examine. If the correct word (061_80 is indeed there, set the computer to run. This will cause the Altair to begin execution of the monitor. On the Teletype the word READY will appear. There are five possible responses which the user may give after carriage return <CR> is pressed: 1) L (load octal), 2) D (dump octal), 3) T (load paper tape), 4) P (punch paper tape), and 5) G (execute the program called). To all of these commands the response at the TTY will be S ?, which is a request for the starting address. Commands D and P will also request an ending address by typing E ? after the starting address has been specified and <CR> pressed. The format for specifying an address is LLL-HHH where LLL are the three low order octal digits and HHH are the three high order octal digits. The address must be followed by a carriage return.

To load octal information into the computer from the TTY one need only input the starting address (after typing L and <CR>, then one may type up to eight octal words per line (separated by one and only one character) followed by <CR>. The monitor will specify the current address you are loading into every eighth word. When finished loading the program, one must type <CTRL> X which will return control to the system monitor. At anytime that the monitor is waiting for input you may type <CTRL> X which will return the monitor to the READY state. The only exception to this is when the T command has been employed. After a tape has been read in one must manually restart the monitor by pressing the stop/run switch on the Altair to stop, pressing examine 100_8, and then run.

The monitor occupies locations $100\text{-}000_8$ through $350\text{-}002_8$. The data acquisition program is also on paper tape as is the output routine; these occupy $340\text{-}002_8$ through $070\text{-}004_8$ and $000\text{-}005_8$ through $070\text{-}005_8$ respectively.

Procedure for Single Sweep Mode and Signal Time Averaging: The interface units are connected in the manner illustrated in Figure 3-1 to provide for data acquisition. It is important to make sure that all grounds are common and connected back to the power supply. It is not necessary to ground any of the actual module containers since all grounds are floating. Spectral information, as Figure 3-1 indi-

Figure 3-1 System interconnections of computer/interface for time averaging and single scan storage.


25 CONNECTOR CABLE
ANALOG AMPLIFIER
AND A/D CONVERTER
SIGNAL INPUT
S1
S2
S3
VR1
VR2
GND
+15
-15
+5
ADC ENABLE (GREEN)
PARALLEL I/O
SERIAL I/O
25 CONNECTOR CABLE
TELETYPE
ALTAIR 8800
MICROPROCESSOR
SWITCH DEBOUNCE 5V SUPPLY
+5V
GND
CLOCK OUT
PROGRAMMABLE CLOCK
ADC ENABLE
RAMP OUTPUT
CLOCK IN
+5
-15
+15
GND
DIGITAL SWEEPER
ORANGE COAX
PLUG P5 ON NMR'S DIGITAL SWEEP BOARD
REAR PANEL OF NMR
GND
SIGNAL OUT. TERMINAL
NMR SPECTROMETER
ORANGE COAX
+5V
-15V
+15V
GND.
GND.
RED
YELLOW
WHITE
BLACK
BLACK
POWER SUPPLY

cates, is monitored at the signal output terminals on the rear panel of the NMR.

There are several adjustments to the interfacing modules and the NMR that must be made prior to their use in single or multi sweep storage. After the usual sample preparation the specimen should be placed in the NMR and a rough idea of the concentration obtained by seeing if a spectrum can be produced by the standard procedure. If spectral information can be obtained on the chart recorder then low amplification (X1 to X100) is desired. By referring to Table 2-1 the appropriate switch combinations and approximate potentiometer settings should be made on the analog amplifier module. If no spectral information can be obtained then the analog amplifier should be set for a higher initial gain, (e.g., $X10^2$ to $X10^4$). It should be noted that the NMR's amplitude control setting only effects the recorder response and does not change the gain at the signal output terminals on the NMR's rear panel.

An oscilloscope (set for low speed scan) should now be connected to the test point on the analog amplifier module, and the microtoggle set to the TEST POINT position. The input leads to the module should be plugged into the signal output banana jacks on the rear panel of the NMR.

A second approximation of the correct amplifier setting may now be obtained by putting the NMR into the 7.5 second

continuous sweep mode, (press SET, turn REC/CRO to CRO, and turn on NMR's oscilloscope to visually monitor). Turning the system power supply on should cause vertical deflection to begin on the oscilloscope that is connected to the test point. If no changing deflection is observed and instead, the signal appears to be locked or either positive or negative 25 v with respect to ground, then the amplifier gain must be reduced until the signal is no longer locked. After the gain has been reduced and spectral information begins to appear on the oscilloscope screen, the offset adjust of the amplifier may be carefully varied while simultaneously increasing the amplifier gain (the offset adjust is internal and requires a thin screw-driver).

One the proper gain has been achieved to "unlock" the signal, the offset should be adjusted so that the base of the signal information (and noise) rests on 0 v (relative ground) and the highest of the positive going peaks are at 10 v.

A final check of the amplitude and offset adjustments should be made by sweeping through the spectrum at the normal 155 second rate. In most cases the offset will not need adjustment, but amplifier gain will probably have to be increased somewhat*.

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* Another adjustment which occasionally should be checked is the D/A offset. Chapter II section B outlines the method of adjustment.

Placing the microtoggle switch in the ADC position now places the analog signal at the analog input port of the converter. A major reason for the above procedure was to protect the A/D from too high an input signal which could permanently damage this rather expensive component.

If TMS (tetramethylsilane) has been added to the sample and a long time averaging run is going to be made it might be advisable to adjust the TMS peak to 0 ppm with the 50 Hz shift button depressed. When data acquisition is about to start the 50 Hz button may be released thus shifting TMS 50 Hz upfield and out of the spectral region to be scanned. It should be noted that the external sweeper does not interfere with the operation of the expanded scale and shift features of the NMR; thus these features may also be used during time averaging.

The interfacing modules and the NMR are now ready for link-up with the computer. Once the data acquisition program has been loaded (see T command above and associated monitor restart instructions) it may be called by pressing G on the TTY and then <CR> followed by the starting address of the program (340-002), <CR>. Program execution will begin, causing the following request to appear on the TTY: INPUT NUMBER OF RAMPS - IN OCTAL PLEASE?. This number must be a power of two and in octal code. Thus the following responses will yield the specified number of ramps:

000_8 = 1 ramp

002_8 = 2 ramps

004_8 = 4 ramps

010_8 = 8 ramps

020_8 = 16 ramps

040_8 = 32 ramps

100_8 = 64 ramps

200_8 = 128 ramps

400_8 = 256 ramps

The maximum number of scans that the averaging system can manage, assuming a 10 volt input to the A/D which corresponds to a signal peak (and thus is coherent), is 256. This can be understood by realizing that a 10 volt input to the A/D will cause the output word (8 bits) to be all 1's. Since the program stores in double precision the maximum number of times that 2^8 can be stored is 2^8 times = 256; a larger number of ramps in such a case would result in memory overflow, and thus a reduction in the significance of the data.

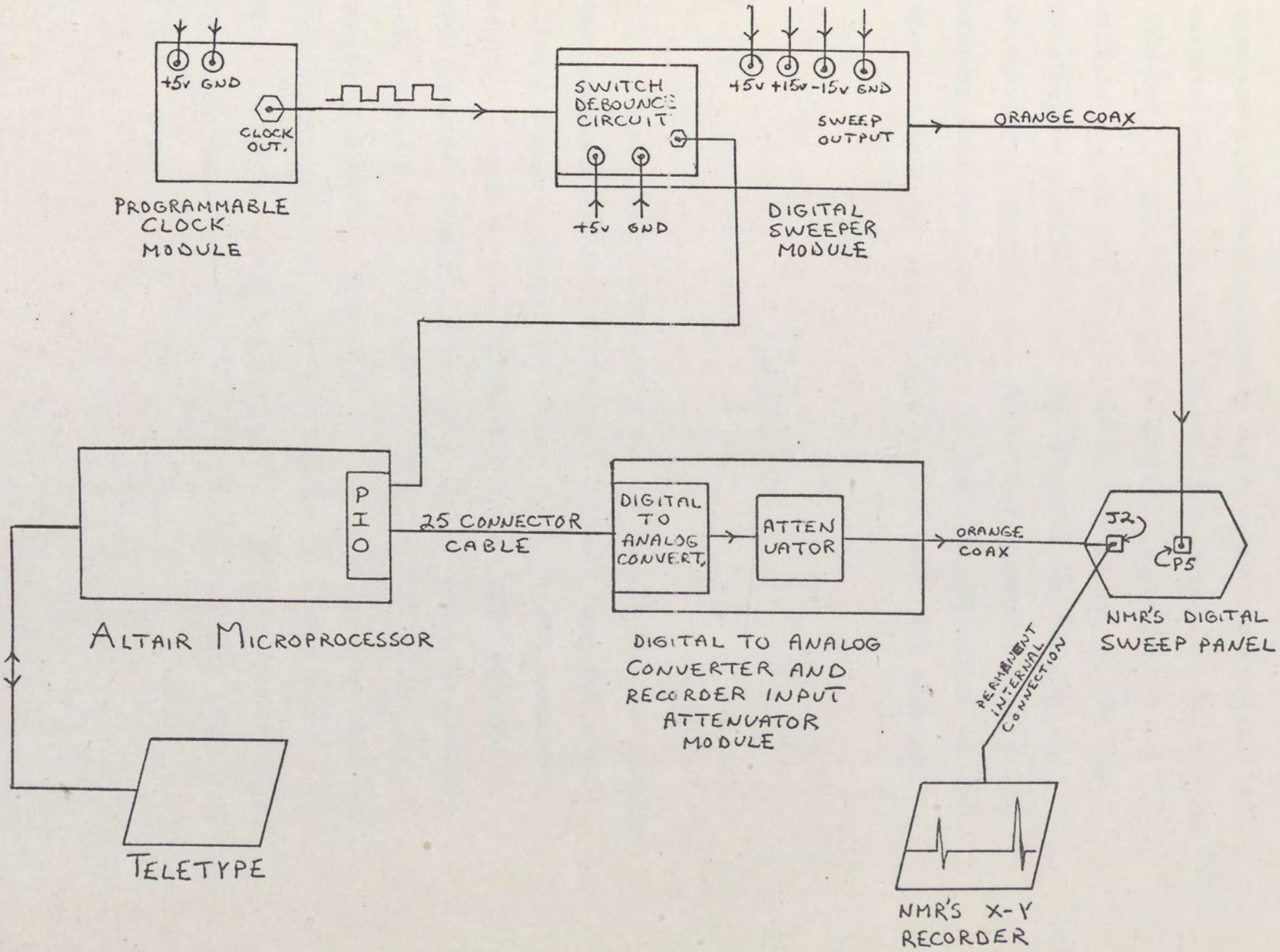
Once the number of ramps have been specified carriage return (<CR>) should be typed and the program will then wait for the first ready signal from the ADC. Throwing the RELEASE switch on the sweep generator module will cause data acquisition to begin.

During program execution, when data is being stored, the pressing of any key on the TTY will result in program halt, and re-initialization of the memory table to its first position. This routine allows for the checking of the amplifier offset (which can change due to thermal drift) and the tuning of the NMR during a long averaging run.

When the specified number of runs have been completed all memory locations will be divided by the number of ramps and the result tranferred to the paper tape punch on the TTY, which will print out the binary equivalent of the contents of each of the 1024 storage channels.

Output Program and Procedure: To transfer the binary coded spectral data to the NMR's X-Y recorder requires a few changes in the interface module interconnections (see Figure 3-2). Specifically the 25 pin data cable must be removed from the amplifier/signal digitizer module and plugged into the digital to analog converter/recorder input attenuator module. The ADC enable line on the digital sweeper module must be tied to the SBO line on the recorder input module. In addition power connections to the amplifier module should be transferred to the attenuator module since the amplifier/digitizer part of the system is not needed to return data to the recorder. Finally the output of the attenuator module must be connected to J2 on the NMR's digital sweeper panel.

Figure 3-2 System interconnections for the transfer of data from computer memory back to the NMR's recorder.


+5v GND
CLOCK OUT.
PROGRAMMABLE CLOCK MODULE
SWITCH DEBOUNCE CIRCUIT
+5v +15v -15v GND
SWEEP OUTPUT
+5v GND
DIGITAL SWEEPER MODULE
ORANGE COAX
P I O
25 CONNECTOR CABLE
ALTAIR MICROPROCESSOR
DIGITAL TO ANALOG CONVERT.
ATTEN UATOR
DIGITAL TO ANALOG CONVERTER AND RECORDER INPUT ATTENUATOR MODULE
ORANGE COAX
J2
P5
NMR'S DIGITAL SWEEP PANEL
PERMANENT INTERNAL CONNECTION
TELETYPE
NMR'S X-Y RECORDER

The output program is loaded into the Altair in the same way that the acquisition program was transferred. To execute, type G and then the starting address of the program $(000\text{-}005)_8$. Upon carriage return the computer will be waiting for the SBO line to pulse, informing the CPU that data may be transferred to the external device (DAC and attenuator). Throwing the INITIALIZE/RELEASE switch to the RELEASE position will result in the de-digitization of the spectral data and the plotting of the usual NMR spectrum.

B. RESULTS

At the time of the completion of this report the interface-computer system has successfully been used for generating a library spectra with the P.E. R-24A NMR spectrometer. A zerox of the binary coded paper tape of a TMS/$CHCl_3$ in CCl_4 sample ($\sim$ 10% $CHCl_3$ v/v) is shown in Figure 3-3. Table 3-1 is the octal coded equivalent of the 1024 storage locations. The table is read from left to right and consists of two octal coded words per memory location. Since the program reduces the double precision data to an 8 bit word, the upper order 8 bits of each location appears as 000.

Figure 3-3 Zerox of binary coded paper tape of TMS/ $CHCl_3$ spectrum, (10% v/v).

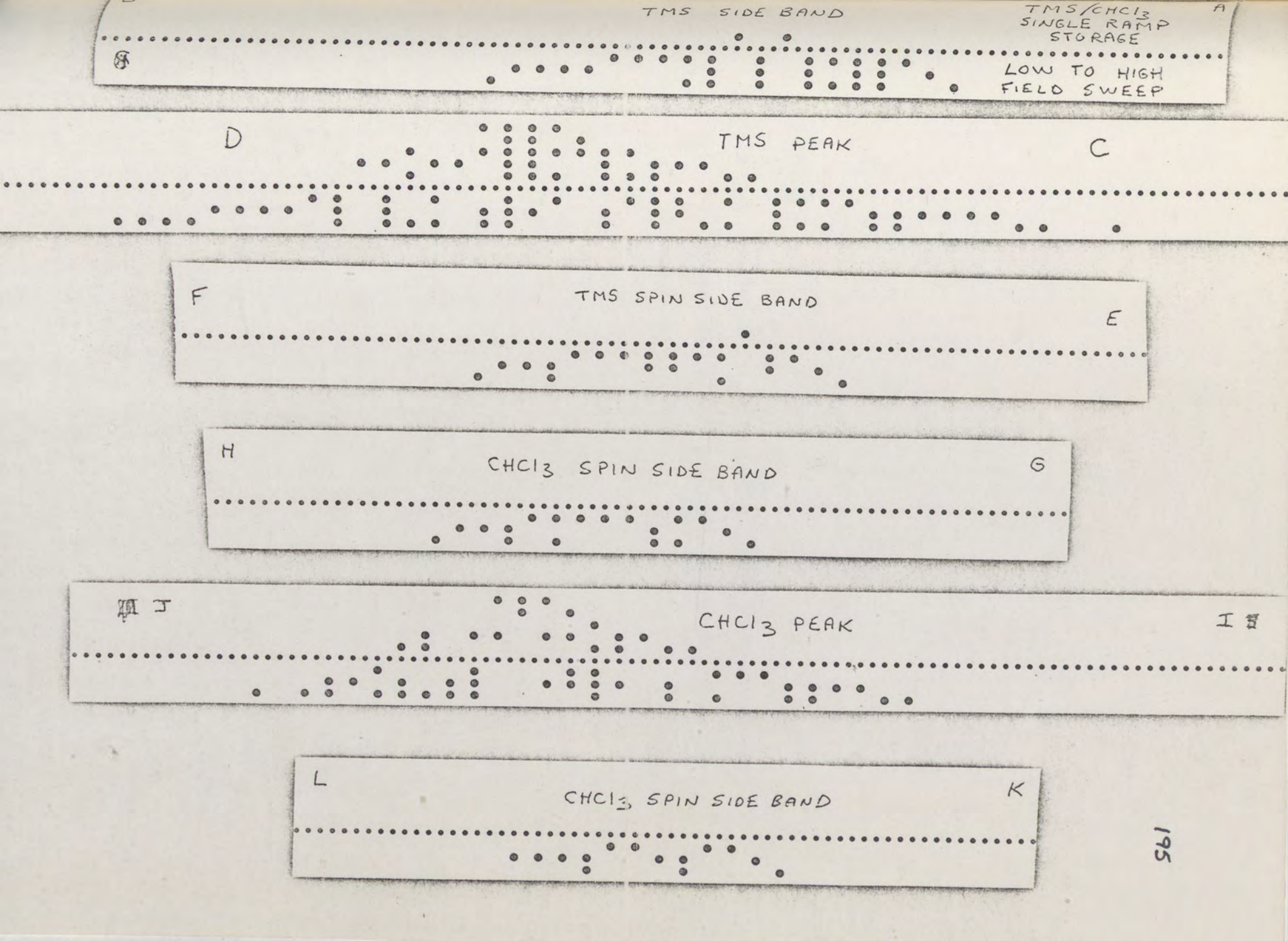

TMS SIDE BAND
TMS/CHCl3
SINGLE RAMP
STORAGE
A
LOW TO HIGH
FIELD SWEEP
D
TMS PEAK
C
F
TMS SPIN SIDE BAND
E
H
CHCl3 SPIN SIDE BAND
G
J
CHCl3 PEAK
I
L
CHCl3 SPIN SIDE BAND
K

Table 3-1 Octal coded data table of TMS/$CHCl_3$ (10% v/v) produced by the computer at the Teletype terminal.

```
?P

S?000-010

E?000-020
!+GWZ\,
READY

?
READY

?G

S?330-002

INPUT NUMBER OF RAMPS - IN OCTAL PLEASE?000

READY

?P

S?000-010

E?000-020
&;@,Z#)/V@
READY

?D

S?000-010

E?000-020

010-000: 000, 062, 000, 000, 000, 000, 000, 000,
010-010: 000, 000, 000, 000, 000, 000, 000, 000,
010-020: 000, 000, 000, 000, 000, 000, 000, 000,
010-030: 000, 000, 000, 000, 000, 000, 000, 001,
010-040: 000, 002, 000, 004, 000, 007, 000, 007,
010-050: 000, 005, 000, 007, 000, 010, 000, 007,
010-060: 000, 010, 000, 007, 000, 005, 000, 004,
010-070: 000, 004, 000, 004, 000, 002, 000, 002,
010-100: 000, 002, 000, 002, 000, 001, 000, 000,
010-110: 000, 000, 000, 000, 000, 000, 000, 000,
010-120: 000, 000, 000, 000, 000, 000, 000, 000,
010-130: 000, 000, 000, 000, 000, 000, 000, 000,
010-140: 000, 000, 000, 000, 000, 000, 000, 000,
010-150: 000, 000, 000, 000, 000, 000, 000, 000,
010-160: 000, 000, 000, 000, 000, 000, 000, 000,
010-170: 000, 000, 000, 000, 000, 000, 000, 000,
010-200: 000, 000, 000, 001, 000, 000, 000, 000,
010-210: 000, 001, 000, 001, 000, 002, 000, 002,
010-220: 000, 002, 000, 002, 000, 003, 000, 003,
010-230: 000, 004, 000, 005, 000, 005, 000, 007,
010-240: 000, 010, 000, 015, 000, 021, 000, 026,
010-250: 000, 037, 000, 054, 000, 073, 000, 140,
010-260: 000, 254, 000, 372, 000, 377, 000, 243,
010-270: 000, 020, 000, 025, 000, 051, 000, 027,
010-300: 000, 020, 000, 007, 000, 004, 000, 002,
010-310: 000, 002, 000, 002, 000, 002, 000, 001,
010-320: 000, 001, 000, 001, 000, 001, 000, 000,
010-330: 000, 000, 000, 000, 000, 000, 000, 000,
010-340: 000, 000, 000, 000, 000, 000, 000, 000,
010-350: 000, 000, 000, 000, 000, 000, 000, 000,
```

TMS SPIN SIDEBAND

TMS

```
011-010: 000, 000, 000, 000, 000, 000, 000, 000,
011-020: 000, 000, 000, 000, 000, 000, 000, 000,
011-030: 000, 000, 000, 000, 000, 000, 000, 000,
011-040: 000, 000, 000, 000, 000, 000, 000, 000,
011-050: 000, 000, 000, 000, 000, 000, 000, 000,
011-060: 000, 000, 000, 000, 000, 001, 000, 002,
011-070: 000, 004, 000, 006, 000, 010, 000, 005,
011-100: 000, 004, 000, 006, 000, 006, 000, 004,
011-110: 000, 004, 000, 004, 000, 003, 000, 002,
011-120: 000, 002, 000, 001, 000, 000, 000, 000,
011-130: 000, 000, 000, 000, 000, 000, 000, 000,
011-140: 000, 000, 000, 000, 000, 000, 000, 000,
011-150: 000, 000, 000, 000, 000, 000, 000, 000,
011-160: 000, 000, 000, 000, 000, 000, 000, 000,
011-170: 000, 001, 000, 002, 000, 002, 000, 000,
011-200: 000, 000, 000, 000, 000, 000, 000, 000,
011-210: 000, 000, 000, 000, 000, 000, 000, 000,
011-220: 000, 000, 000, 000, 000, 002, 000, 002,
011-230: 000, 002, 000, 000, 000, 000, 000, 000,
011-240: 000, 000, 000, 000, 000, 000, 000, 000,
011-250: 000, 001, 000, 003, 000, 004, 000, 004,
011-260: 000, 004, 000, 002, 000, 002, 000, 002,
011-270: 000, 004, 000, 004, 000, 004, 000, 005,
011-300: 000, 005, 000, 007, 000, 004, 000, 001,
011-310: 000, 002, 000, 001, 000, 000, 000, 001,
011-320: 000, 001, 000, 000, 000, 000, 000, 000,
011-330: 000, 000, 000, 000, 000, 000, 000, 000,
011-340: 000, 000, 000, 000, 000, 000, 000, 000,
011-350: 000, 000, 000, 000, 000, 000, 000, 000,
011-360: 000, 000, 000, 000, 000, 000, 000, 000,
011-370: 000, 000, 000, 000, 000, 000, 000, 000,
012-000: 000, 000, 000, 000, 000, 000, 000, 000,
012-010: 000, 000, 000, 000, 000, 000, 000, 000,
012-020: 000, 000, 000, 000, 000, 000, 000, 000,
012-030: 000, 000, 000, 000, 000, 000, 000, 000,
012-040: 000, 000, 000, 000, 000, 000, 000, 000,
012-050: 000, 000, 000, 000, 000, 000, 000, 000,
012-060: 000, 000, 000, 000, 000, 000, 000, 000,
012-070: 000, 000, 000, 000, 000, 000, 000, 000,
012-100: 000, 000, 000, 000, 000, 000, 000, 000,
012-110: 000, 000, 000, 002, 000, 002, 000, 000,
012-120: 000, 000, 000, 000, 000, 000, 000, 000,
012-130: 000, 000, 000, 000, 000, 000, 000, 000,
012-140: 000, 000, 000, 000, 000, 000, 000, 000,
012-150: 000, 000, 000, 000, 000, 000, 000, 000,
012-160: 000, 000, 000, 000, 000, 000, 000, 000,
012-170: 000, 000, 000, 000, 000, 000, 000, 000,
012-200: 000, 000, 000, 000, 000, 000, 000, 000,
012-210: 000, 000, 000, 000, 000, 000, 000, 000,
012-220: 000, 000, 000, 000, 000, 000, 000, 000,
012-230: 000, 000, 000, 000, 000, 000, 000, 000,
012-240: 000, 000, 000, 000, 000, 000, 000, 000,
012-250: 000, 000, 000, 000, 000, 000, 000, 000,
012-260: 000, 000, 000, 000, 000, 000, 000, 000,
012-270: 000, 000, 000, 000, 000, 000, 000, 000,
012-300: 000, 000, 000, 000, 000, 000, 000, 000,
012-310: 000, 000, 000, 000, 000, 000, 000, 000,
012-320: 000, 000, 000, 000, 000, 000, 000, 000,
012-330: 000, 000, 000, 000, 000, 000, 000, 000,
012-340: 000, 000, 000, 000, 000, 000, 000, 000,
012-350: 000, 000, 000, 000, 000, 000, 000, 000,
012-360: 000, 000, 000, 000, 000, 000, 000, 000,
012-370: 000, 000, 000, 000, 000, 000, 000, 000,
013-000: 000, 000, 000, 000, 000, 000, 000, 000,
```

TMS SPIN SIDE BAND

IMPURITY IN SAMPLE

```
013-030: 000, 000, 000, 000, 000, 000, 000, 000,
013-040: 000, 000, 000, 000, 000, 000, 000, 000,
013-050: 000, 000, 000, 000, 000, 000, 000, 000,
013-060: 000, 000, 000, 000, 000, 000, 000, 000,
013-070: 000, 000, 000, 000, 000, 000, 000, 000,
013-100: 000, 000, 000, 000, 000, 000, 000, 000,
013-110: 000, 000, 000, 000, 000, 000, 000, 000,
013-120: 000, 000, 000, 000, 000, 000, 000, 000,
013-130: 000, 000, 000, 000, 000, 000, 000, 000,
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013-150: 000, 000, 000, 000, 000, 000, 000, 000,
013-160: 000, 000, 000, 000, 000, 000, 000, 000,
013-170: 000, 000, 000, 000, 000, 000, 000, 000,
013-200: 000, 000, 000, 000, 000, 000, 000, 000,
013-210: 000, 000, 000, 000, 000, 000, 000, 000,
013-220: 000, 000, 000, 000, 000, 000, 000, 000,
013-230: 000, 000, 000, 000, 000, 002, 000, 002,
013-240: 000, 001, 000, 000, 000, 000, 000, 000,
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013-260: 000, 000, 000, 000, 000, 002, 000, 002,
013-270: 000, 001, 000, 000, 000, 000, 000, 000,
013-300: 000, 000, 000, 000, 000, 000, 000, 000,
013-310: 000, 000, 000, 000, 000, 000, 000, 000,
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013-330: 000, 000, 000, 000, 000, 000, 000, 000,
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013-350: 000, 000, 000, 000, 000, 000, 000, 000,
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014-070: 000, 000, 000, 000, 000, 000, 000, 000,
014-100: 000, 000, 000, 000, 000, 000, 000, 000,
014-110: 000, 000, 000, 000, 000, 000, 000, 000,
014-120: 000, 000, 000, 000, 000, 000, 000, 000,
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014-140: 000, 000, 000, 000, 000, 000, 000, 000,
014-150: 000, 000, 000, 000, 000, 000, 000, 000,
014-160: 000, 000, 000, 000, 000, 000, 000, 000,
014-170: 000, 000, 000, 000, 000, 000, 000, 000,
014-200: 000, 000, 000, 000, 000, 000, 000, 000,
014-210: 000, 000, 000, 000, 000, 000, 000, 000,
014-220: 000, 000, 000, 000, 000, 000, 000, 000,
014-230: 000, 000, 000, 000, 000, 000, 000, 000,
014-240: 000, 000, 000, 000, 000, 000, 000, 000,
014-250: 000, 000, 000, 000, 000, 000, 000, 000,
014-260: 000, 000, 000, 000, 000, 000, 000, 000,
014-270: 000, 000, 000, 000, 000, 000, 000, 000,
014-300: 000, 000, 000, 000, 000, 000, 000, 000,
014-310: 000, 000, 000, 000, 000, 000, 000, 000,
014-320: 000, 000, 000, 000, 000, 000, 000, 000,
014-330: 000, 000, 000, 000, 000, 000, 000, 000,
014-340: 000, 000, 000, 000, 000, 000, 000, 001,
014-350: 000, 002, 000, 002, 000, 002, 000, 001,
014-360: 000, 000, 000, 000, 000, 000, 000, 000,
014-370: 000, 000, 000, 000, 000, 000, 000, 000,
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015-010: 000, 000, 000, 000, 000, 000, 000, 000,
015-020: 000, 000, 000, 000, 000, 000, 000, 000,
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015-040: 000, 000, 000, 000, 000, 000, 000, 000,
015-050: 000, 000, 000, 000, 000, 000, 000, 000,
015-060: 000, 000, 000, 000, 000, 000, 000, 000,
015-070: 000, 000, 000, 000, 000, 000, 000, 000,
015-100: 000, 000, 000, 000, 000, 000, 000, 000,
015-110: 000, 000, 000, 000, 000, 000, 000, 000,
015-120: 000, 000, 000, 000, 000, 000, 000, 000,
015-130: 000, 000, 000, 000, 000, 000, 000, 000,
015-140: 000, 000, 000, 000, 000, 000, 000, 000,
015-150: 000, 000, 000, 000, 000, 000, 000, 000,
015-160: 000, 002, 000, 002, 000, 002, 000, 000,
015-170: 000, 000, 000, 000, 000, 000, 000, 000,
015-200: 000, 000, 000, 000, 000, 000, 000, 000,
015-210: 000, 000, 000, 000, 000, 000, 000, 000,
015-220: 000, 000, 000, 000, 000, 000, 000, 000,
015-230: 000, 000, 000, 000, 000, 000, 000, 000,
015-240: 000, 000, 000, 000, 000, 000, 000, 000,
015-250: 000, 000, 000, 000, 000, 000, 000, 000,
015-260: 000, 000, 000, 000, 000, 000, 000, 000,
015-270: 000, 000, 000, 000, 000, 000, 000, 000,
015-300: 000, 000, 000, 000, 000, 000, 000, 000,
015-310: 000, 000, 000, 000, 000, 000, 000, 000,
015-320: 000, 000, 000, 000, 000, 000, 000, 000,
015-330: 000, 000, 000, 000, 000, 000, 000, 000,
015-340: 000, 000, 000, 000, 000, 000, 000, 000,
015-350: 000, 000, 000, 000, 000, 000, 000, 000,
015-360: 000, 000, 000, 000, 000, 000, 000, 001,
015-370: 000, 002, 000, 004, 000, 005, 000, 003,
016-000: 000, 004, 000, 004, 000, 004, 000, 005,
016-010: 000, 004, 000, 003, 000, 002, 000, 002,
016-020: 000, 001, 000, 000, 000, 000, 000, 000,
016-030: 000, 000, 000, 000, 000, 000, 000, 000,
016-040: 000, 000, 000, 000, 000, 000, 000, 000,
016-050: 000, 000, 000, 000, 000, 000, 000, 000,
016-060: 000, 000, 000, 000, 000, 000, 000, 000,
016-070: 000, 000, 000, 000, 000, 000, 000, 000,
016-100: 000, 000, 000, 000, 000, 000, 000, 000,
016-110: 000, 000, 000, 000, 000, 000, 000, 000,
016-120: 000, 000, 000, 000, 000, 000, 000, 000,
016-130: 000, 000, 000, 000, 000, 000, 000, 000,
016-140: 000, 000, 000, 001, 000, 001, 000, 002,
016-150: 000, 002, 000, 003, 000, 003, 000, 004,
016-160: 000, 004, 000, 005, 000, 010, 000, 013,
016-170: 000, 020, 000, 032, 000, 057, 000, 126,
016-200: 000, 222, 000, 300, 000, 220, 000, 027,
016-210: 000, 003, 000, 031, 000, 013, 000, 005,
016-220: 000, 002, 000, 003, 000, 001, 000, 000,
016-230: 000, 001, 000, 000, 000, 000, 000, 000,
016-240: 000, 000, 000, 000, 000, 000, 000, 000,
016-250: 000, 000, 000, 000, 000, 000, 000, 000,
016-260: 000, 000, 000, 000, 000, 000, 000, 000,
016-270: 000, 000, 000, 000, 000, 000, 000, 000,
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016-310: 000, 000, 000, 000, 000, 000, 000, 000,
016-320: 000, 000, 000, 000, 000, 000, 000, 000,
016-330: 000, 000, 000, 000, 000, 000, 000, 000,
016-340: 000, 000, 000, 000, 000, 000, 000, 000,
016-350: 000, 000, 000, 000, 000, 000, 000, 000,
016-360: 000, 000, 000, 000, 000, 000, 000, 000,
016-370: 000, 000, 000, 000, 000, 000, 000, 000,
017-000: 000, 000, 000, 000, 000, 000, 000, 001,
017-010: 000, 002, 000, 004, 000, 004, 000, 003,
017-020: 000, 002, 000, 004, 000, 004, 000, 003,
017-030: 000, 002, 000, 002, 000, 002, 000, 000,
017-040: 000, 000, 000, 000, 000, 000, 000, 000,

$CHCl_3$ SPIN SIDE BAND

$CHCl_3$

$CHCl_3$ SPIN SIDE BAND

```
017-060: 000, 000, 000, 000, 000, 000, 000, 000,
017-070: 000, 000, 000, 000, 000, 000, 000, 000,
017-100: 000, 000, 000, 000, 000, 000, 000, 000,
017-110: 000, 000, 000, 000, 000, 000, 000, 000,
017-120: 000, 000, 000, 000, 000, 000, 000, 000,
017-130: 000, 000, 000, 000, 000, 000, 000, 000,
017-140: 000, 000, 000, 000, 000, 000, 000, 000,
017-150: 000, 000, 000, 000, 000, 000, 000, 000,
017-160: 000, 000, 000, 000, 000, 000, 000, 000,
017-170: 000, 000, 000, 000, 000, 000, 000, 000,
017-200: 000, 000, 000, 000, 000, 000, 000, 000,
017-210: 000, 000, 000, 000, 000, 000, 000, 000,
017-220: 000, 000, 000, 002, 000, 002, 000, 003,
017-230: 000, 003, 000, 001, 000, 000, 000, 000,
017-240: 000, 000, 000, 000, 000, 000, 000, 000,
017-250: 000, 000, 000, 000, 000, 000, 000, 000,
017-260: 000, 000, 000, 000, 000, 000, 000, 000,
017-270: 000, 000, 000, 000, 000, 000, 000, 000,
017-300: 000, 000, 000, 000, 000, 000, 000, 000,
017-310: 000, 000, 000, 000, 000, 000, 000, 000,
017-320: 000, 000, 000, 000, 000, 000, 000, 000,
017-330: 000, 000, 000, 000, 000, 000, 000, 000,
017-340: 000, 000, 000, 000, 000, 000, 000, 000,
017-350: 000, 000, 000, 000, 000, 000, 000, 000,
017-360: 000, 000, 000, 000, 000, 000, 000, 000,
017-370: 000, 000, 000, 000, 000, 000, 000, 000,
020-000: 377,
READY

?
```

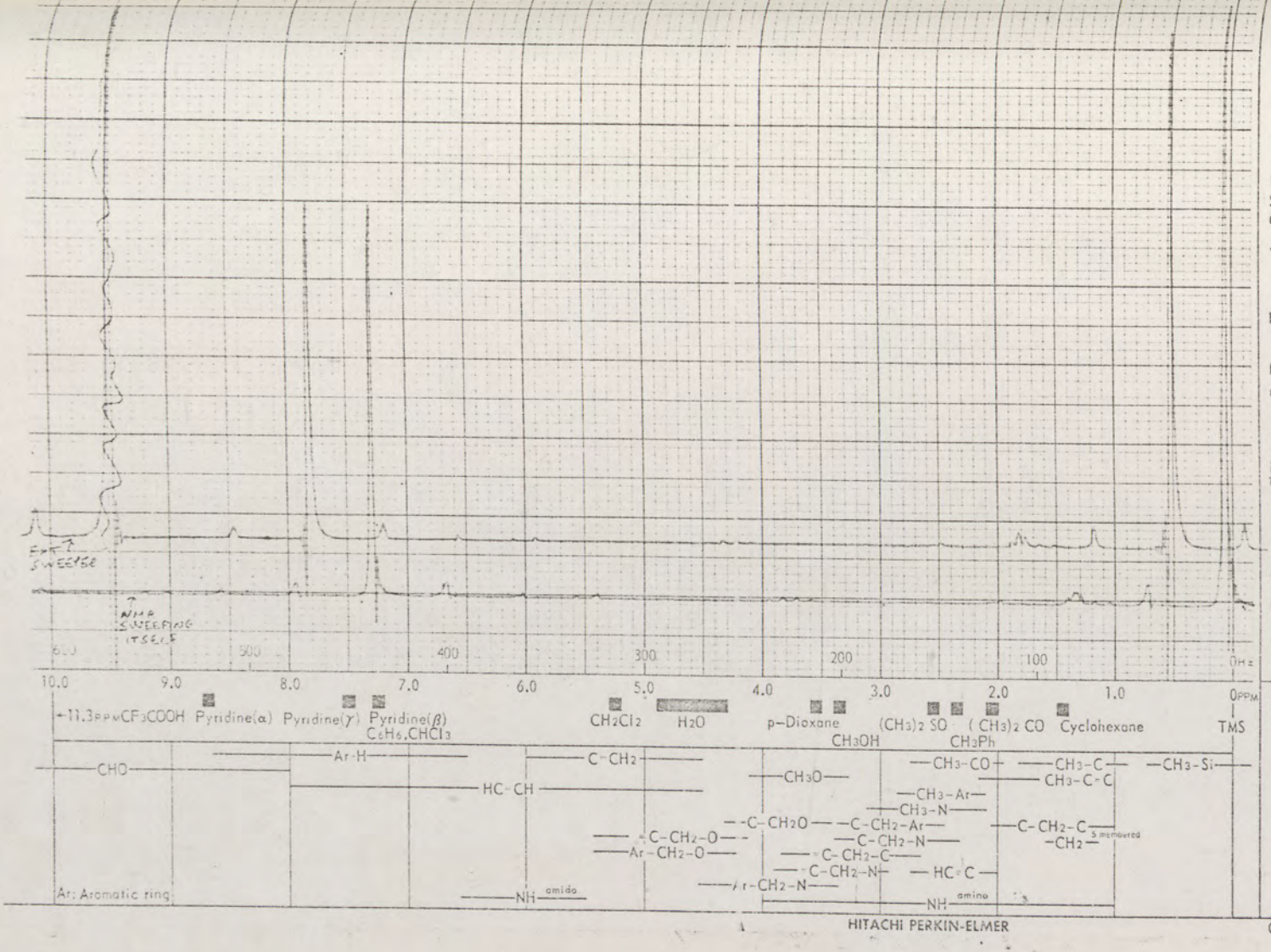
A visual comparison between a TMS/$CHCl_3$ spectrum as produced by X axis sweeping with the NMR's sweep circuit, and the spectrum as it appears when the external digital ramping circuit controls the NMR, is contained in Figure 3-4. The lower spectrum was swept by the NMR's internal circuitry; the upper scan was produced by the digital sweeper module. There is a slight offset of 0.3 ppm downfield for the externally produced sweep which can easily be compensated for (if need be) by adjusting the TMS position control on the NMR.

The storage of the digitized data and its subsequent retrieval via the paper tape is proof of the proper operation of the power supply, digital sweep, clock, and amplifier/digitizer modules as well as the computer portion of the interface.

Presently the recorder interface to the computer is nearing completion; this will allow the plotting of the stored data on the NMR's recorder unit. The output program has been written, and is contained in Appendix 2-3.

Time averaging has not as of yet been performed because of programming difficulties; however the problems are only minor and should soon be corrected. It is important to note that the price of commercially available time averaging equipment is on the order of $10,000.00. Our system cost under $1300.00 (see Table 3-2) and is adaptable to a wide

Figure 3-4 NMR spectrum of TMS/$CHCl_3$ (10% v/v) as swept by the NMR (lower spectrum) vs. the externally controlled sweep (upper spectrum).



REFFERENCE:
SOLVENT:
CONC:
AMPLITUDE:
SPECTRUM
INTEGRAL
H1 LEVEL:
HI | NOR | LO
H2 LEVEL:
GAIN:
X1 | X10
SWEEP WIDTH:
NOR SCALE EXP.
10PPM 600 500 400 300 200 100 0
SHIFT
50Hz | 50Hz | 50Hz
SWEEP TIME
☐ 300/150 SEC ☐ / SEC
DATE:
OPERATOR

REMARKS:
Correlation test for internal vs. external sweep position – #1
B/A adjustment of D/A offset

HITACHI PERKIN-ELMER
CHART NO. 435-7204 PRINTED IN U.S.A.

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Table 3-2 Cost break-down for the computer/interface system.

PART	NUMBER	PRICE
Unipolar Digital to Analog Converter	DAC-10Z-1	$ 49.00
A/D Converter	ADC-EH8B1	85.00
D/A Converter Bipolar	DAC-10Z-3	49.00
Assorted Gates, Counters, Flip-Flops, Op-Amps, Power Regulators		25.00
Transformers		10.00
Vector Boards		5.00
Sockets		15.00
Potentiometers		10.00
Switches, Resistors, Capacitors		5.00
Cabinets		12.00
Miscellaneous		5.00
Altair Microprocessor with Serial I/O and Parallel I/O	8800	1000.00
TOTAL		1270.00

range of both data acquisition and instrument control applications due to the modular construction of the interface and the incorporation of a complete digital microprocessor.

C. FUTURE APPLICATIONS

Gas Chromatography: The analog output of a gas chromatograph may be connected to the multi-purpose computer interface for a variety of data processing jobs. Initially, as in the NMR experiment, the analog output must be boosted to the input requirements of the ADC. Once the digital data has begun entering the computer processing may begin. One of the simplest routines would be the calculation of individual peak areas via an algorithm based on the establishment of a signal threshold; integration would begin when the computer senses that the incoming data is above the predetermined threshold level, and it would end when the value of the data drops below the threshold value. Integration can be accomplished by the Altair through the utilization of a double precision addition routine, the resultant value of which would be proportional to the peak area[61]. Obviously the selection of the threshold value would be critical in such a routine. If it were set too high small

peaks might be missed; if set too low noise could trigger the integration process. In addition, a finite error would be introduced in all peaks since the small area corresponding to the threshold area would be missing from the calculated area. To reduce the effects of noise a consistency test could be included in the program which would reject data that was not (for a set number of data points) consistently above or below the threshold level*.

The computer may also be programmed to calculate retention times. A rather simple method would involve a program which would recognize a consistently sharp increase and decrease of the values of the incoming data. A computer routine could then determine the largest value in between the change in slope. Since all data goes sequentially into a designated block of memory, the address location of the maximum would yield the retention time knowing what the data acquisition rate is.

As with time averaging, data acquisition from the GC is much slower than the operating speed of the computer. Thus the computer could be used to control experimental conditions as a result of the instantaneous evaluation of the

---

* A simple program for GC peak integration can be found in reference 61, p. 54. This reference also contains an excellant bibliography of computer to chemical instrumentation interfaces, p. 338.

incoming data. The computer could be used to change column temperature as well as the output amplification factor of the detector during the experimental run. Continuous Teletype or chart recorder printout can also be obtained, thus allowing the user to monitor the chromatogram before an entire chromatogram is taken.

Overlapping peaks and non-zero base lines can also be dealt with by computer algorithms; the reader is referred to references 62 through 65 for more complete information.

The modular computer/interface system is readily adaptable to GC data acquisition. The mV output of the detector amplifier circuitry, which is normally applied to the Y axis of a sensitive chart recorder, may instead be tied to the input line of the analog amplifier and analog to digital module. The amplifier portion of the module will boost the mV signal levels to the 0 to 10 v input requirements of the A/D. The output lines of the converter as with the NMR, applied to the parallel I/O board of the computer.

The digital output lines from the PIO can be used to trigger relays which will cause servo motors to change such parameters as manifold and injector part temperatures. The PIO output lines could also be used to monitor the information as it is being acquired. This would be accomplished through the use of the digital to analog converter and recorder input attenuator module, the output of which could be tied to the Y axis input of a chart recorder.

UV-Visible spectroscopy is another area in which computer control and data processing is applicable. The Cary 118 UV-Vis. spectrometer is a digitally oriented instrument in that wavelength drive and Y axis shift with respect to changing detector output is monitored and controlled to a great extent by digital circuits. The operating manual for the Cary 118 details those timing and control pulses which are available for external control and monitoring. Among these functions are absorbance and percent transmittance range selection (e.g., 0 to 100% T, 0 to 1 Abs., etc.), absorbance zero suppression selection and mode selection (single beam, auto gain or auto slit). Ordinary TTL logic levels of 0 and +5v are used to control the selection procedure; thus the Cary 118 is fully compatible with the interface/computer electronics.

The Cary 118 uses a digital panel meter for the continuous display of either absorbance, % transmittance or concentration. The connector to this meter carries the binary coded decimal (BCD) equivalent of the photometric measurement data. The connector also contains two programmable 'read data' lines, which allow the user the option of 4 readings per second, 30 readings per second, or a variable rate line (open to read, ground to hold). Neither amplification or conversion of these signals is necessary; thus these output lines may be directly attached to parallel I/O parts on the Altair.

Digital computer control of scan rates and direction are easily accomplished with the Cary 118. Repetitive scans over selected spectral ranges can, therefore, be performed. Kinetics and cyclical studies would be greatly simplified through the use of such an arrangement.

The possible applications of micro-computers in the chemical laboratory are quite extensive. Table 3-3 is a brief listing of some of the applications. The limits are truly those of the imagination.

1. Data acquisition and processing
2. File search, pattern recognition, curve fitting
3. Display-TTY, CRT, plotter (raw or correlated data)
4. Instrument automation
5. Real time computer interaction (such as NMR time averaging)
6. Iterative optimization of experiments
7. User-computer interactive experimentation

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APPENDIX 1

220

Series 54/74

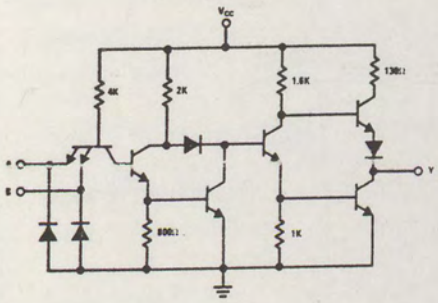
DM5408/DM7408(SN5408/SN7408) quad 2-input AND gate
DM5409/DM7409(SN5409/SN7409) quad 2-input AND gate (open collector)

general description

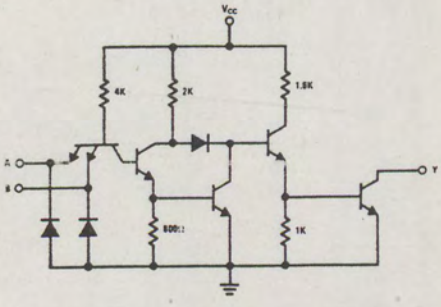
The DM5408/DM7408 and DM5409/DM7409 provide the non-inverting AND function in the popular quad 2-input pin configuration.

schematic and connection diagrams

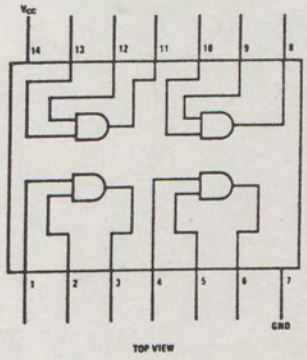
DM5408, DM7408



DM5409, DM7409



Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5408, DM5409	4.5	5.5	V
DM7408, DM7409	4.75	5.25	V
Temperature (T_A)			
DM5408, DM5409	−55	+125	°C
DM7408, DM7409	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Voltage DM5408/DM7408	V_{CC} = Min, V_{IN} = 2V, I_{OUT} = −800 μA	2.4			V
Logical "1" Output Current DM5409/DM7409	V_{CC} = Min, V_{OUT} = 5.5V, V_{IN} = 2.0V			250	μA
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 0.8V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
	V_{CC} = Max, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Output Short Circuit Current (Note 3)	V_{CC} = Max DM5408	−20		−55	mA
	V_{CC} = Max DM7408	−18		−55	mA
Supply Current — Logical "1" (each device)	V_{CC} = Max, V_{IN} = 5V		11	21	mA
Logical "0"	V_{CC} = Max, V_{IN} = 0V		20	33	mA
Input Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA		−1.0	−1.5	V
Propagation Delay to a Logical "0" from DM5408/DM7408 Any Input to Output, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C		14	19	ns
Propagation Delay to a Logical "0" from DM5409/DM7409 Any Input to Output, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C		15	24	ns
Propagation Delay to a Logical "1" from DM5408/DM7408 Any Input to Output, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C		13	27	ns
Propagation Delay to a Logical "1" From DM5409/DM7409 Any Input to Output, t_{pd1}	V_{CC} = 5.0V, T_A = 25°C		17	32	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5408, DM5409 and across the 0°C to 70°C range for the DM7408, DM7409. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Series 54/74

DM5432/DM7432(SN5432/SN7432) quad 2-input OR gate

general description

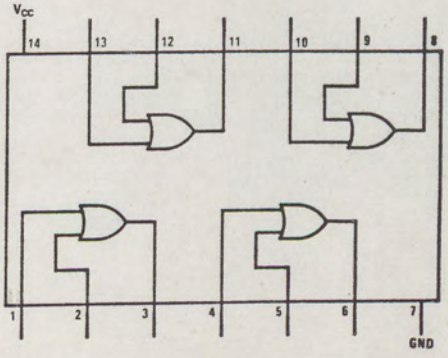
The DM5432/DM7432 (SN5432/SN7432) is a quad 2-input OR gate utilizing TTL (Transistor-Transistor Logic) to provide the basic functions used in the implementation of digital integrated circuit systems. The device is completely compatible with all other Series 54/74 devices.

features

- Popular digital logic block
- Saves inverter function when sign inversion is not needed

logic and connection diagram

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Operating Temperature Range	
DM7032	−55°C to 125°C
DM8032	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM5432 / DM7432	V_{CC} = 4.5V / V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	DM5432 / DM7432	V_{CC} = 4.5V / V_{CC} = 4.75V			.8	V
Logical "1" Output Voltage	DM5432 / DM7432	V_{CC} = 4.5V / V_{CC} = 4.75V, V_{IN} = 2.0V, I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	DM5432 / DM7432	V_{CC} = 4.5V / V_{CC} = 4.75V, V_{IN} = .8V, I_{OUT} = 16 mA			.4	V
Logical "1" Input Current	DM5432 / DM7432	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 2.4V			40	μA
	DM5432 / DM7432	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM5432 / DM7432	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 0.4V		−1.0	−1.6	mA
Output Short Circuit Current (Note 3)	DM5432 / DM7432	V_{CC} = 5.5V / V_{CC} = 5.25V	−20 / −18	−32	−55	mA
Supply Current – Logical "1" (Each Device)	DM5432 / DM7432	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 5.0V Each Gate			4.4	mA
Logical "0"	DM5432 / DM7432	V_{CC} = 5.5V / V_{CC} = 5.25V, V_{IN} = 0V Each Gate			8.8	mA
Input Clamp Voltage		V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA		−1.0	−1.5	V
Propagation Delay to a Logical "0", t_{pd0}		V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω	5	15	22	ns
Propagation Delay to a Logical "1", t_{pd1}		V_{CC} = 5.0V, T_A = 25°C, C_L = 50 pF, R_L = 400Ω	5	12	18	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5432 and across the 0°C to 70°C range for the DM7432. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Gates, Series 54/74

DM7400 (SN7400) quadruple two-input NAND gate
DM7410 (SN7410) triple three-input NAND gate
DM7420 (SN7420) dual four-input NAND gate

general description

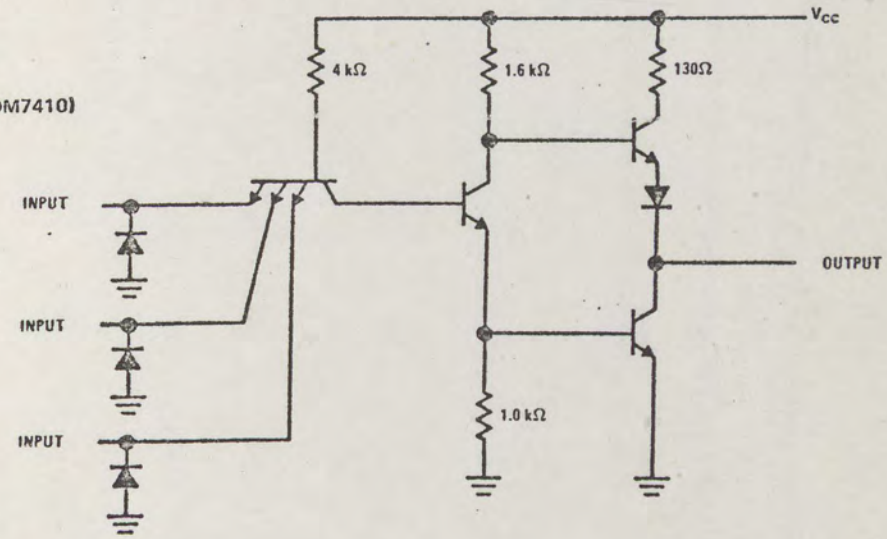
Employing TTL (Transistor-Transistor-Logic) to achieve high speed at moderate power dissipation, these gates provide the basic functions used in the implementation of digital integrated circuit systems. Characteristics of the circuits include high noise immunity, low output impedance, good capacitive drive capability, and minimal variation in switching times with temperature. The gates are compatible with and interchangeable with Series 74 equivalent.

Key features include:

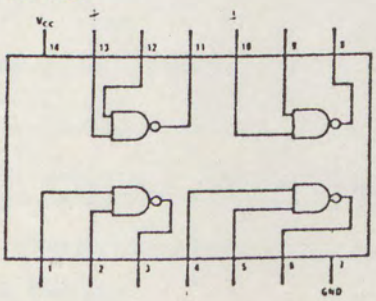
- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan Out 10
- Allowable Power Supply Variation 4.75V to 5.25V
- Average Propagation Delay 13 ns
- Average Power Dissipation 10 mW per gate

schematic and connection diagrams

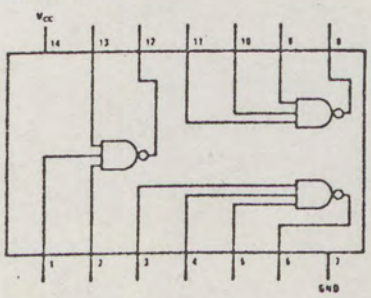
(shown for DM7410)



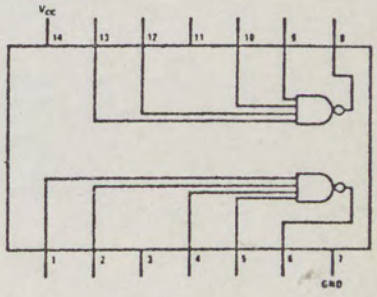
DM7400



DM7410



DM7420



absolute maximum ratings

Vcc	7.0V
Input Voltage	5.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Fan-Out	10
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	V_{CC} = 4.75V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage	V_{CC} = 4.75V V_{IN} = 0.8V, I_{OUT} = −400μA	2.4			V
Logical "0" Output Voltage	V_{CC} = 4.75V V_{IN} = 2.0V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = 5.25V V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = 5.25V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = 5.25V V_{IN} = 0.4V			−1.6	mA
Output Short Circuit Current (Note 2)	V_{CC} = 5.25V V_{IN} = 0V	−18		−55	mA
Supply Current— Logical "0" (Note 3)	V_{CC} = 5.25V V_{IN} = 5.0V		3	5.1	mA
Supply Current— Logical "1" (Note 3)	V_{CC} = 5.25V V_{IN} = 0V		1	1.8	mA
Propagation Delay Time to Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		8	15	ns
Propagation Delay Time to Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C, C = 50 pF		13	25	ns

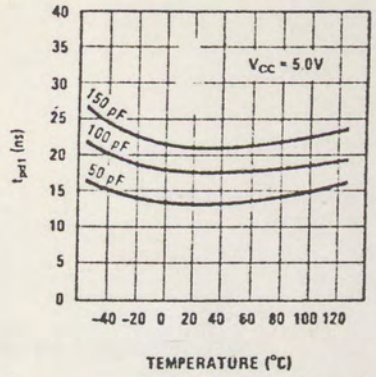
Note 1: Min/max limits apply across the guaranteed temperature range 0°C to 70°C unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Not more than 1 output should be shorted at a time.

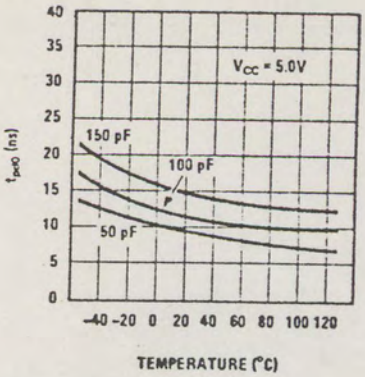
Note 3: Each gate.

typical performance characteristics

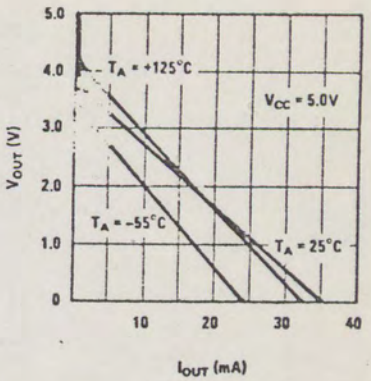
Transition Time to a Logical "1" (t_{pd1}) vs Temperature



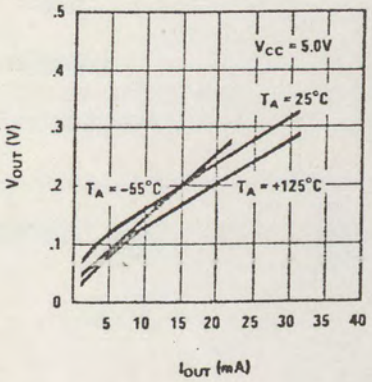
Transition Time to a Logical "0" (t_{pd0}) vs Temperature



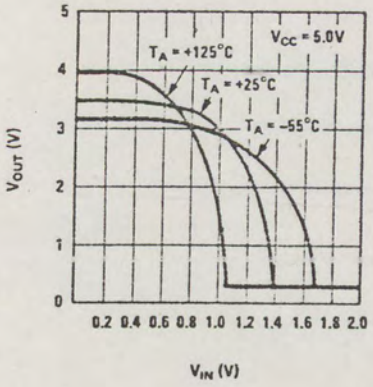
Logical "1" Output Voltage vs Source Current



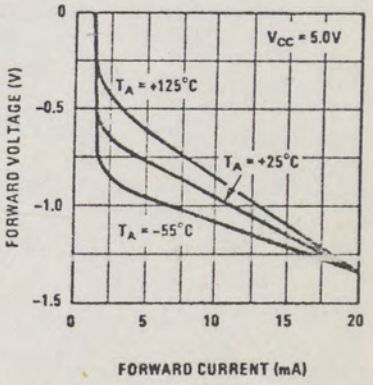
Logical "0" Output Voltage vs Sink Current



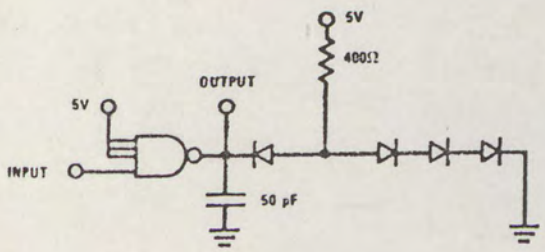
V_{IN} vs V_{OUT}



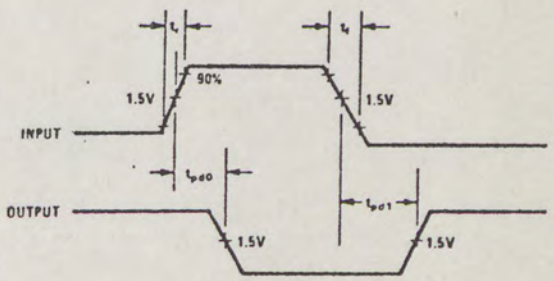
Input Clamp Diode Characteristics



ac test circuit



switching time waveform



$t_r = t_f = 10\ \mu s$
pw = 100 ns
frequency = 1 MHz
V_{CC} = 5.0V

Gates, Series 54/74

DM5404/DM7404 (SN5404/SN7404) hex inverter

general description

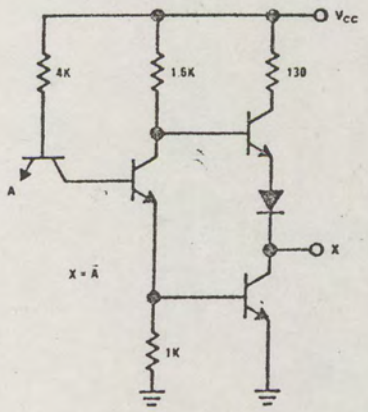
The DM5404/DM7404 is a hex inverter utilizing TTL to achieve high speed at nominal power dissipation. It is totally compatible with other Series 54/74 devices.

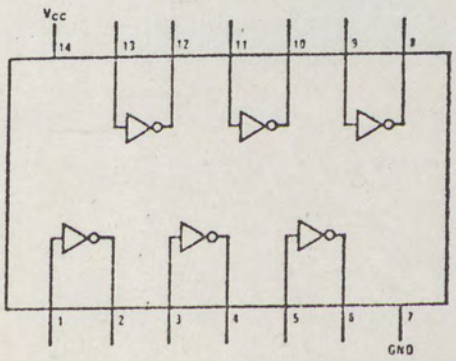
Features include:

- Input clamping diodes
- Typical Noise Immunity 1V
- Guaranteed Noise Immunity 400 mV
- Fan-out 10
- Allowable Power Supply Variation
  - DM5404 4.5V to 5.5V
  - DM7404 4.75V to 5.25V
- Average Propagation Delay 12 ns (with 50 pF)
- Average Power Dissipation 10 mW per gate

schematic and connection diagrams

DM5404/DM7404





absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Operating Temperature Range	
DM7404	0°C to 70°C
DM5404	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 1)

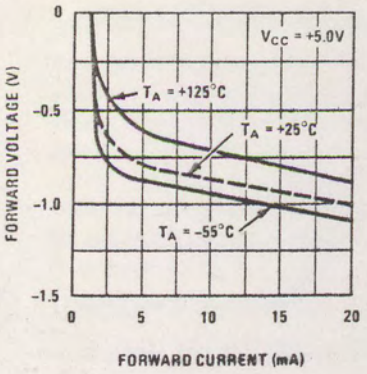
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Input diode clamp voltage		V_{CC} = 5.0V, I_{IN} = −12 mA	T_A = 25°C			−1.5	V
Logical "1" Input Voltage	DM5404	V_{CC} = 4.5V		2.0			V
	DM7404	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM5404	V_{CC} = 4.5V				0.8	V
	DM7404	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM5404	V_{CC} = 4.5V	V_{IN} = 0.8V, I_{OUT} = −400 μA	2.4			V
	DM7404	V_{CC} = 4.75V					
Logical "0" Output Voltage	DM5404	V_{CC} = 4.5V	V_{IN} = 2.0V, I_{OUT} = 16 mA			0.4	V
	DM7404	V_{CC} = 4.75V					
Logical "1" Input Current	DM5404	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM7404	V_{CC} = 5.25V					
Logical "1" Input Current	DM5404	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM7404	V_{CC} = 5.25V					
Logical "0" Input Current	DM5404	V_{CC} = 5.5V	V_{IN} = 0.4V		−1.0	−1.6	mA
	DM7404	V_{CC} = 5.25V					
Output Short Circuit Current (Note 2)	DM5404	V_{CC} = 5.5V	V_{OUT} = 0	−20	−30	−55	mA
	DM7404	V_{CC} = 5.25V		−18			
Supply Current - Logical "0" (each gate)	DM5404	V_{CC} = 5.5V					
	DM7404	V_{CC} = 5.25V	V_{IN} = 5.0V		3.0	5.1	mA
Supply Current - Logical "1" (each gate)	DM5404	V_{CC} = 5.5V	V_{IN} = 0		1.0	1.8	mA
	DM7404	V_{CC} = 5.25V					
Propagation Delay to a Logical "1", t_{pd1}		T_A = 25°C, N = 10	V_{CC} = 5.0V, C = 50 pF	5	16	22	ns
Propagation Delay to a Logical "0" t_{pd0}		T_A = 25°C, N = 10	V_{CC} = 5.0V, C = 50 pF	3	9	15	ns

Note 1. Min/Max limits apply across the guaranteed temperature range of 0°C to 70°C for the DM7404, and −55°C to +125°C for the DM5404, unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

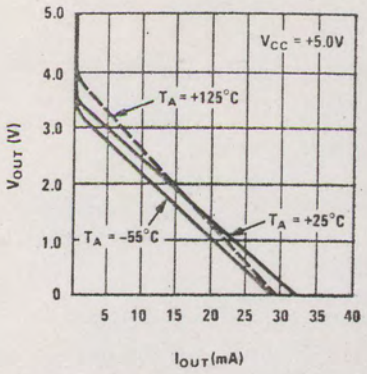
Note 2. Only one output at a time should be short circuited.

typical performance characteristics

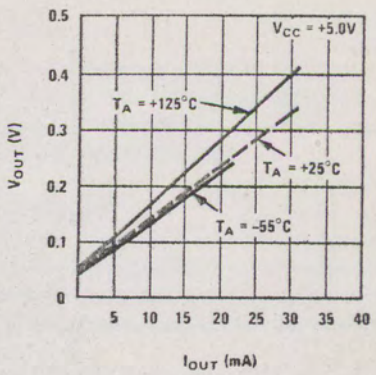
Input Clamp Diode Characteristics



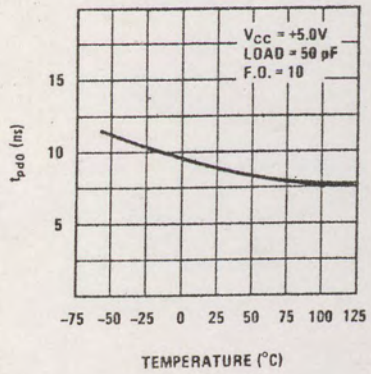
Logical "1" Output Voltage vs Source Current



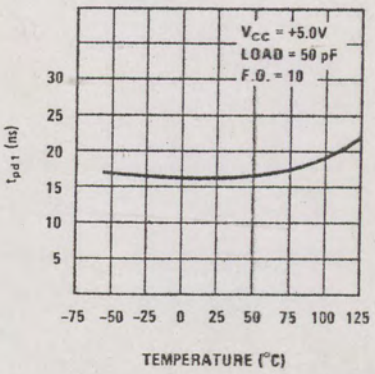
Logical "0" Output Voltage vs Sink Current



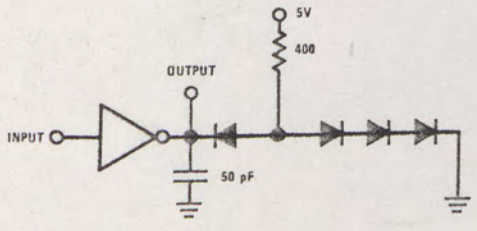
Transition Time to a Logical "0", t_{pd0} vs Temperature



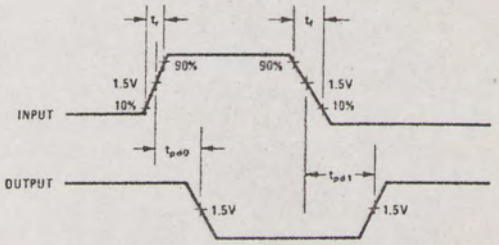
Transition Time to a Logical "1", t_{pd1} vs Temperature



ac test circuit



switching time waveform



$t_r = t_f$ = 10 ns
pw = 100 ns
frequency = 1 MHz
V_{CC} = 5.0V

DM7520/DM8520 modulo-n divider

general description

The DM7520/DM8520 combines TTL technology and MSI (Medium Scale Integration) design to provide a circuit equal in complexity to more than 50 gates.

Although extremely versatile in a number of digital applications, its primary usage will be realized in two areas:

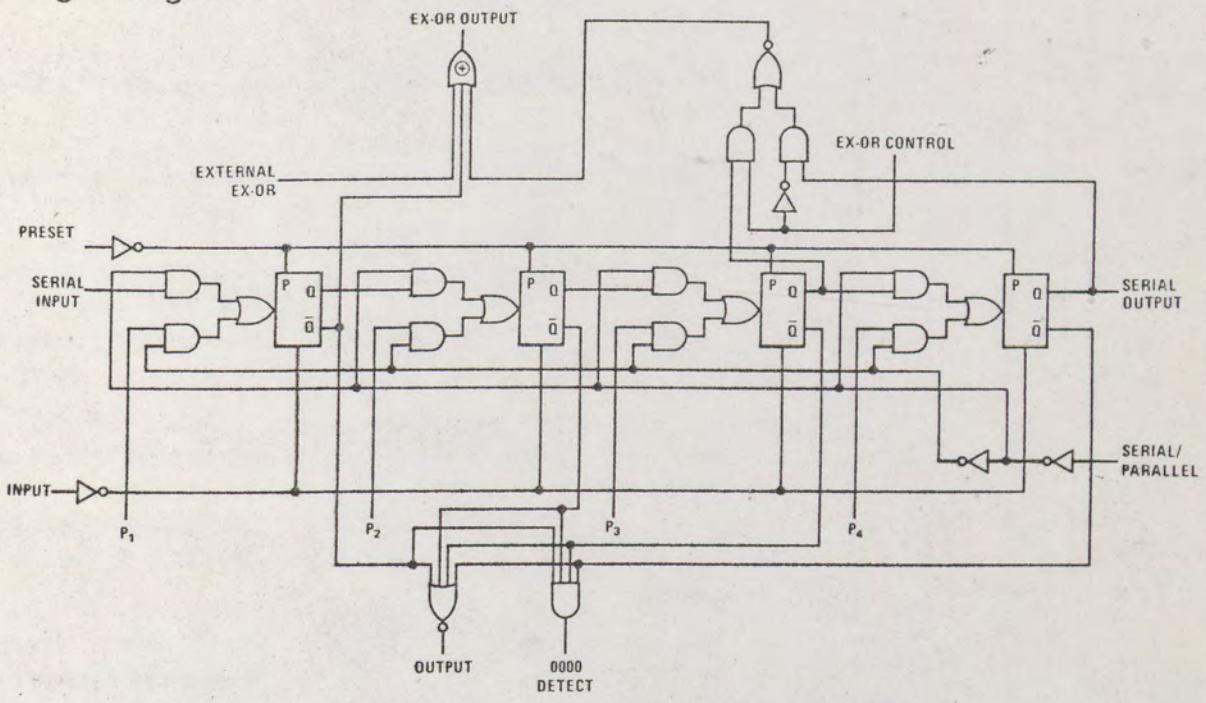
1. MODULO-N DIVIDER

   A single DM7520/DM8520 can be programmed without external components to divide by any number from 2 to 15. Cascading of these dividers will provide division by any number from 2 to very large numbers.

2. SHIFT REGISTER

   Since the basic organization of the logic is that of a serial shift register, the device may be used where four-bit parallel-in-serial out shifting is required.

logic diagram



connection diagram

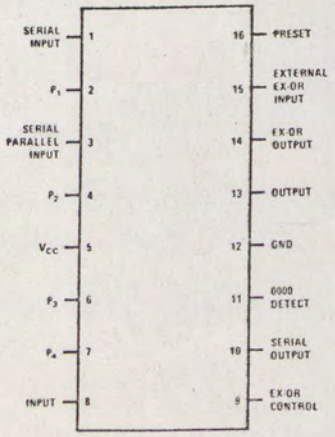


table for division by n

SETTING P_1	P_2	P_3	P_4	÷BY
1	1	1	0	2
1	1	0	0	3
1	0	0	0	4
0	0	0	1	5
0	0	1	0	6
0	1	0	0	7
1	0	0	1	8
0	0	1	1	9
0	1	1	0	10
1	1	0	1	11
1	0	1	0	12
0	1	0	1	13
1	0	1	1	14
0	1	1	1	15

231

absolute maximum ratings

Supply Voltage		7V
Input Voltage		5.5V
Operating Temperature Range	DM7520	−55°C to +125°C
	DM8520	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		300°C

electrical characteristics (Note 1)

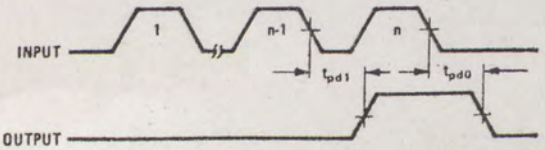
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7520	V_{CC} = 4.5V					
	DM8520	V_{CC} = 4.75V		2.0			V
Logical "0" Input Voltage	DM7520	V_{CC} = 4.5V					
	DM8520	V_{CC} = 4.75V				0.8	V
Logical "1" Output Voltage	DM7520	V_{CC} = 4.5V					
	DM8520	V_{CC} = 4.75V	I_{OUT} = −400 μA	2.4			V
Logical "0" Output Voltage	DM7520	V_{CC} = 4.5V					
	DM8520	V_{CC} = 4.75V	I_{OUT} = 16 mA			0.4	V
Logical "0" Input Current (All inputs except pin 9)	DM7520	V_{CC} = 5.5V					
	DM8520	V_{CC} = 5.25V	V_{IN} = 0.4V			1.6	mA
Logical "0" Input Current (Pin 9)	DM7520	V_{CC} = 5.5V					
	DM8520	V_{CC} = 5.25V	V_{IN} = 0.4V			3.2	μA
Logical "1" Input Current	DM7520	V_{CC} = 5.5V					
	DM8520	V_{CC} = 5.25V	V_{IN} = 2.4V			40	μA
Logical "1" Input Current (Pin 9)	DM7520	V_{CC} = 5.5V					
	DM8520	V_{CC} = 5.25V	V_{IN} = 2.4V			80	μA
Logical "1" Input Current (All inputs except pin 9)	DM7520	V_{CC} = 5.5V					
	DM8520	V_{CC} = 5.25V	V_{IN} = 5.5V			1	mA
Output Short Circuit Current (Note 3)	DM7520	V_{CC} = 5.5V		−20			
	DM8520	V_{CC} = 5.25V	V_{OUT} = 0V (Note 2)	−18		55	mA
Power Supply Current		V_{CC} = 5.0V	T_A = 25°C		50		mA
Counting Frequency		V_{CC} = 5.0V	T_A = 25°C		20		MHz

Note 1: Unless otherwise specified, limits shown apply across the −55°C to +125°C temperature range for the DM7520 and the 0°C to +70°C temperature range for the DM8520. Typical values apply to supply voltages of 5.0V.

Note 2: Only one output should be shorted at a time.

Note 3: Serial and exclusive OR outputs.

switching time waveforms



theory of operation

The basic operation of the DM7520/DM8520 is derived from the fact that when several outputs of a shift register are EXCLUSIVE OR'ed and the result fed back to the register's input, a unique progression of stable states results on the outputs of the flip-flops. Depending upon which outputs are EXCLUSIVE OR'ed the number of different states can be varied. Even if optimum gating is provided the most states which can be obtained is 2^n-1, where n is equal to the number of flip-flops in the register. The all-zero state is precluded; and, therefore, the maximum number of states is always one less than the theoretical maximum number. Since the DM7520/DM8520 contains four flip-flops, its maximum number of states is 15. Because the 1111 state occurs only once during a 15-state sequence, this state is detected; and its output becomes the output of the divider.

To obtain frequency division by numbers other than the maximum, it is necessary to cause the register to "jump" immediately from its initial 1111 to the state which it would normally reach in 16-m (m = desired frequency division) pulses. For example, to divide by eleven it would be necessary to jump to the fifth state and then simply allow the register to normally progress forward to its original state. The output of the divider is also used as a control pulse. Since the 1111 state is detected and since the "jump-state" information is of interest only at the time that this state is reached, the OUTPUT is used to gate the parallel inputs, through the SERIAL/PARALLEL input, so that it recognizes this "jump-state" information only at this time. Subsequently as the states change, the parallel input information is locked from the divider.

Should the divider ever be accidently set in the forbidden 0000 state, an output is provided to detect this state. If this output is in turn fed into the EXTERNAL EX-OR input, a 1 will be forced into the register at the next clock pulse, thus clearing the unallowed state.

A PRESET input is provided which when taken to a logical "1" level overrides all other inputs and sets the register to the 1111 state.

To divide by numbers greater than 15, it is necessary to cascade DM7520/DM8520's. Both the OUTPUT and the 0000 DETECT output are capable of being connected directly to other like outputs thus providing the "WIRED-OR" configuration. These outputs should be connected to the similar outputs on other dividers for proper operation. All SERIAL/PARALLEL inputs should be connected to the common OUTPUT.

Other connections are shown. (Figure 1 indicates connections for 2 dividers or a maximum frequency division of 255. For division by higher numbers, a more complete discussion of the interconnection techniques will be given in the final data sheet.)

To divide by numbers between 16 and 255, the table in Figure 2 will apply.

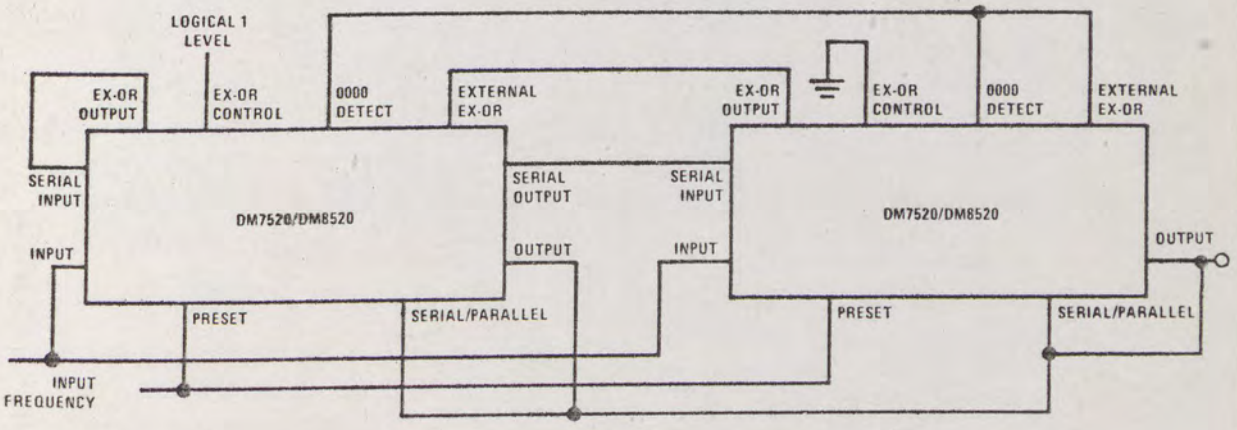


FIGURE 1. Connection for 2 Divider or Maximum Frequency Division of 255

SETTING								÷ BY
DIVIDER 1				DIVIDER 2				
P_1	P_2	P_3	P_4	P_1	P_2	P_3	P_4	
0	1	1	1	1	1	1	1	255
1	0	1	1	1	1	1	1	254
0	1	0	1	1	1	1	1	253
0	0	1	0	1	1	1	1	252
1	0	0	1	0	1	1	1	251
0	1	0	0	1	0	1	1	250
0	0	1	0	0	1	0	1	249
0	0	0	1	0	0	1	0	248
0	0	0	0	1	0	0	1	247
0	0	0	0	0	1	0	0	246
0	0	0	0	0	0	1	0	245
0	0	0	0	0	0	0	1	244
1	0	0	0	0	0	0	0	243
1	1	0	0	0	0	0	0	242
1	1	1	0	0	0	0	0	241
0	1	1	1	0	0	0	0	240
1	0	1	1	1	0	0	0	239
1	1	0	1	1	1	0	0	238
0	1	1	0	1	1	1	0	237
0	0	1	1	0	1	1	1	236
0	0	0	1	1	0	1	1	235
0	0	0	0	1	1	0	1	234
0	0	0	0	0	1	1	0	233
0	0	0	0	0	0	1	1	232
1	0	0	0	0	0	0	1	231
0	1	0	0	0	0	0	0	230
0	0	1	0	0	0	0	0	229
1	0	0	1	0	0	0	0	228
1	1	0	0	1	0	0	0	227
0	1	1	0	0	1	0	0	226
1	0	1	1	0	0	1	0	225
0	1	0	1	1	0	0	1	224
0	0	1	0	1	1	0	0	223
0	0	0	1	0	1	1	0	222
0	0	0	0	1	0	1	1	221
0	0	0	0	0	1	0	1	220
1	0	0	0	0	0	1	0	219
1	1	0	0	0	0	0	1	218
0	1	1	0	0	0	0	0	217
1	0	1	1	0	0	0	0	216
0	1	0	1	1	0	0	0	215
1	0	1	0	1	1	0	0	214
1	1	0	1	0	1	1	0	213
1	1	1	0	1	0	1	1	212
0	1	1	1	0	1	0	1	211
0	0	1	1	1	0	1	0	210
0	0	0	1	1	1	0	1	209
0	0	0	0	1	1	1	0	208
1	0	0	0	0	1	1	1	207
0	1	0	0	0	0	1	1	206
1	0	1	0	0	0	0	1	205
1	1	0	1	0	0	0	0	204
1	1	1	0	1	0	0	0	203
1	1	1	1	0	1	0	0	202
0	1	1	1	1	0	1	0	201
0	0	1	1	1	1	0	1	200
1	0	0	1	1	1	1	0	199
0	1	0	0	1	1	1	1	198
0	0	1	0	0	1	1	1	197
0	0	0	1	0	0	1	1	196
1	0	0	0	1	0	0	1	195
1	1	0	0	0	1	0	0	194
1	1	1	0	0	0	1	0	193
0	1	1	1	0	0	0	1	192
0	0	1	1	1	0	0	0	191
0	0	0	1	1	1	0	0	190
1	0	0	0	1	1	1	0	189
0	1	0	0	0	1	1	1	188
1	0	1	0	0	0	1	1	187
1	1	0	1	0	0	0	1	186
0	1	1	0	1	0	0	0	185
0	0	1	1	0	1	0	0	184
1	0	0	1	1	0	1	0	183
0	1	0	0	1	1	0	1	182
0	0	1	0	0	1	1	0	181
1	0	0	1	0	0	1	1	180
0	1	0	0	1	0	0	1	179
0	0	1	0	0	1	0	0	178
1	0	0	1	0	0	1	0	177
1	1	0	0	1	0	0	1	176
1	1	1	0	0	1	0	0	175
0	1	1	1	0	0	1	0	174
1	0	1	1	1	0	0	1	173
0	1	0	1	1	1	0	0	172
1	0	1	0	1	1	1	0	171
1	1	0	1	0	1	1	1	170
0	1	1	0	1	0	1	1	169
1	0	1	1	0	1	0	1	168
1	1	0	1	1	0	1	0	167
0	1	1	0	1	1	0	1	166

SETTING								÷ BY
DIVIDER 1				DIVIDER 2				
P_1	P_2	P_3	P_4	P_1	P_2	P_3	P_4	
1	0	1	1	0	1	1	0	165
0	1	0	1	1	0	1	1	164
0	0	1	0	1	1	0	1	163
1	0	0	1	0	1	1	0	162
1	1	0	0	1	1	0	1	161
1	1	1	0	0	1	0	1	160
0	0	0	1	1	0	1	0	159
0	1	1	1	1	0	0	1	158
1	0	1	1	1	0	0	0	157
1	1	0	1	1	1	1	0	156
0	1	1	0	1	1	1	1	155
1	0	1	0	1	1	1	0	154
1	1	0	1	1	1	0	1	153
1	1	1	0	1	1	0	0	152
0	1	1	1	1	1	0	1	151
1	0	1	1	1	1	0	1	150
1	1	0	1	1	1	0	0	149
0	1	1	0	1	1	1	0	148
0	0	1	1	0	1	1	1	147
1	0	0	0	1	1	1	1	146
1	0	0	0	0	1	0	1	145
0	1	1	0	0	0	1	0	144
1	0	1	1	0	0	0	1	143
1	1	0	1	1	0	0	0	142
0	1	1	0	1	1	0	0	141
0	0	1	1	0	1	1	0	140
1	0	0	1	1	0	1	1	139
1	1	0	0	1	1	0	1	138
0	1	1	0	0	1	1	0	137
1	0	1	1	0	0	1	1	136
0	0	1	1	1	0	0	1	135
1	0	0	1	1	1	0	0	134
0	1	0	0	1	1	1	0	133
1	0	1	0	0	1	1	1	132
1	1	0	1	0	0	1	1	131
1	1	1	0	1	0	0	1	130
0	1	1	1	0	1	0	0	129
0	0	1	1	1	0	1	0	128
1	0	0	1	1	1	0	1	127
0	1	0	1	0	1	1	0	126
0	0	1	0	1	0	1	1	125
1	0	1	0	1	0	1	1	124
0	1	0	0	1	0	1	0	123
0	0	1	0	1	0	0	1	122
1	0	0	1	0	1	0	0	121
1	1	0	0	1	0	1	0	120
0	1	1	0	0	1	0	1	119
0	0	1	1	0	0	1	0	118
1	0	0	1	1	0	0	1	117
1	1	0	0	1	1	0	0	116
0	1	1	0	0	1	1	0	115
1	0	1	1	0	0	1	1	114
1	1	0	1	1	0	0	1	113
1	1	1	0	1	1	0	0	112
1	1	1	1	0	1	1	0	111
0	1	1	1	1	0	1	1	110
1	0	1	1	1	1	0	1	109
0	1	0	1	1	1	1	0	108
1	0	1	0	1	1	1	1	107
0	1	0	1	0	1	1	1	106
1	0	1	0	1	0	1	1	105
0	1	0	1	0	1	0	1	104
1	0	1	0	1	0	1	0	103
1	1	0	1	0	1	0	1	102
0	1	1	0	1	0	1	0	101
0	0	1	1	0	1	0	1	100
0	0	0	1	1	0	1	0	99
1	0	0	0	1	1	0	1	98
1	1	0	0	0	1	1	0	97
1	1	1	0	0	0	1	1	96
1	0	1	0	0	1	1	0	95
1	1	1	1	0	0	0	0	94
1	1	1	1	1	0	0	1	93
1	1	1	1	1	1	1	0	92
0	1	0	1	0	1	0	1	91
1	0	1	0	1	0	1	0	90
1	0	0	0	1	0	1	0	89
0	1	0	0	0	1	0	1	88
1	0	1	0	0	0	1	0	87
0	1	0	1	0	0	0	1	86
1	0	1	0	1	0	0	0	85
1	1	0	1	0	1	0	0	84
1	1	1	0	1	0	1	0	83
1	1	1	1	0	1	0	1	82
1	1	1	1	1	0	1	0	81
1	1	1	1	1	1	0	1	80
0	1	1	1	1	1	1	0	79
1	0	0	1	1	1	1	1	78
1	0	0	1	1	1	1	1	77
1	1	0	0	1	1	1	0	76

SETTING								÷ BY
DIVIDER 1				DIVIDER 2				
P_1	P_2	P_3	P_4	P_1	P_2	P_3	P_4	
1	1	1	0	0	1	1	1	75
1	1	1	1	0	0	1	1	74
1	1	1	1	1	0	0	1	73
0	1	1	1	1	1	0	0	72
0	0	1	1	1	1	1	0	71
0	0	0	1	1	1	1	1	70
0	0	0	0	1	1	1	1	69
0	0	0	0	0	1	1	1	68
1	0	0	0	0	0	1	1	67
0	1	0	0	0	0	0	1	66
1	0	1	0	0	0	0	0	65
0	1	0	1	0	0	0	0	64
0	0	1	0	1	0	0	0	63
0	0	0	1	0	1	0	0	62
0	0	0	0	1	0	1	0	61
1	0	0	0	0	1	0	1	60
0	1	0	0	0	0	1	0	59
0	0	1	0	0	0	0	1	58
0	0	0	1	0	0	0	0	57
0	0	0	0	1	0	0	0	56
1	0	0	0	0	1	0	0	55
1	1	0	0	0	0	1	0	54
1	1	1	0	0	0	0	1	53
1	1	1	1	0	0	0	0	52
0	1	1	1	1	0	0	0	51
0	0	1	1	1	1	0	0	50
0	0	0	1	1	1	1	0	49
1	0	0	0	1	1	1	1	48
1	1	0	0	0	1	1	1	47
0	1	1	0	0	0	1	1	46
0	0	1	1	0	0	0	1	45
0	0	0	1	1	0	0	0	44
1	0	0	0	1	1	0	0	43
0	1	0	0	0	1	1	0	42
0	0	1	0	0	0	1	1	41
0	0	0	1	0	0	0	1	40
1	0	0	0	1	0	0	0	39
0	1	0	0	0	1	0	0	38
0	0	1	0	0	0	1	0	37
1	0	0	1	0	0	0	1	36
0	1	0	0	1	0	0	0	35
1	0	1	0	0	1	0	0	34
0	1	0	1	0	0	1	0	33
0	0	1	0	1	0	0	1	32
1	0	0	1	0	1	0	0	31
1	1	0	0	1	0	1	0	30
0	1	1	0	0	1	0	1	29
0	0	1	1	0	0	1	0	28
1	0	0	1	1	0	0	1	27
0	1	0	1	0	1	0	0	26
1	0	1	0	1	1	0	1	25
1	1	0	1	1	0	0	0	24
1	1	1	0	1	1	0	1	23
0	1	1	1	0	1	1	0	22
0	0	1	1	1	0	1	1	21
1	0	0	1	1	1	0	1	20
0	1	0	0	1	1	1	0	19
0	0	1	0	0	1	1	1	18
1	0	0	1	0	0	1	1	17
0	1	0	0	1	0	0	1	16
1	0	1	0	1	0	1	1	15
0	1	0	1	0	1	0	1	14
1	0	1	0	1	0	1	0	13
1	1	0	1	0	1	0	1	12
0	1	1	0	1	0	1	0	11
0	0	1	1	0	1	0	1	10
0	0	0	1	1	0	1	0	9
1	0	0	0	1	1	0	1	8
1	1	0	0	0	1	1	0	7
1	1	1	0	0	0	1	1	6
1	1	1	1	0	0	0	1	5
1	1	1	1	1	0	0	0	4
1	1	1	1	1	1	0	0	3
1	1	1	1	1	1	1	0	2

FIGURE 2. DM7520/8520 Shift Register Divider Input Coding Table (2 Package Combinations)

Series 54L/74L

DM54L192/DM74L192(SN54L192/SN74L192)
up-down decade counter

DM54L193/DM74L193(SN54L193/SN74L193)
up-down binary counter

general description

The DM54L192/DM74L192 and DM54L193/DM74L193 are up-down decade and up-down binary counters respectively. Separate clock inputs determine up or down counting. The unused clock input must be tied high when not in use.

Asynchronous clear and load inputs with clear override provide for parallel data entry. Clear overrides the load as far as asynchronous data entry is concerned. Carry and borrow outputs are controlled synchronously. Normal synchronous operation requires clear = "0" and load = 1.

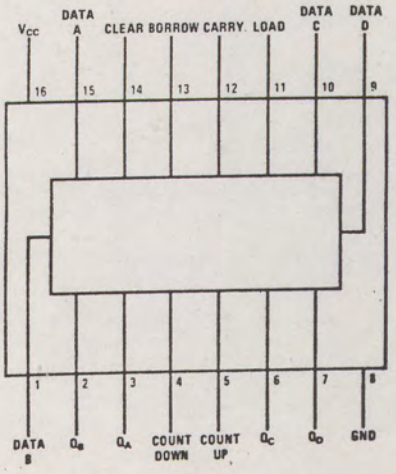
The counters can drive two standard TTL loads over the commercial temperature range and 10 and 20 low power TTL loads in the "0" and "1" states respectively over the military temperature range.

features

- Series 54L/74L compatible
- 40 mW typical power dissipation
- 50 ns typical propagation delay

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Note 1)

Supply Voltage	8.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54L192, DM54L193	4.5	5.5	V
DM74L192, DM74L193	4.75	5.25	V
Temperature (T_A)			
DM54L192, DM54L193	−55	+125	°C
DM74L192, DM74L193	0	70	°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		V_{CC} = Min		2.0	1.3		V
Logical "0" Input Voltage		V_{CC} = Min			1.3	0.7	V
Logical "1" Output Voltage		V_{CC} = Min	I_{OUT} = −200 μA	2.4	2.8		V
Logical "0" Output Voltage	DM54L192,DM54L193	V_{CC} = 4.5V	I_{OUT} = 2 mA		0.15	0.3	V
	DM74L192,DM74L193	V_{CC} = 4.75V	I_{OUT} = 3.6 mA		0.20	0.4	V
Logical "1" Input Current		V_{CC} = Max, V_{IN} = 2.4V			<1	10	μA
		V_{CC} = Max, V_{IN} = 5.5V			<1	100	μA
Logical "0" Input Current		V_{CC} = Max, V_{IN} = 0.3V			−0.10	−0.18	mA
Output Short Circuit Current (Note 3)		V_{CC} = Max, V_{OUT} = 0V		−3	−9	−15	mA
Supply Current I_{CC} Max	DM54L192/DM74L192	V_{CC} = Max			8.0	13	mA
	DM54L193/DM74L193	V_{CC} = Max			7.5	12.5	mA
Propagation Delay to a Logical "0" from Either Count Input to Output, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		75	150	ns
Propagation Delay to a Logical "0" from Count Up to Carry, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		60	120	ns
Propagation Delay to a Logical "1" from Either Count Input to Output, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		45	90	ns
Propagation Delay to a Logical "1" from Count Up to Carry, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		30	60	ns
Maximum Clock Frequency		V_{CC} = 5.0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF	6	12		MHz
Propagation Delay to Logical "1" from Count Down to Borrow, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		30	60	ns
Propagation Delay to Logical "0" from Count Down to Borrow, t_{pd0}		V_{CC} = 5.0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		50	100	ns
t_{SETUP} – Minimum Input Setup		V_{CC} = 5.0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		5	30	ns
Minimum Clock Pulse Width		V_{CC} = 5.0V, T_A = 25°C	R_L = 4 kΩ, C_L = 50 pF		35	70	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54L192, DM54L193 and across the 0°C to 70°C range for the DM74L192, DM74L193. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

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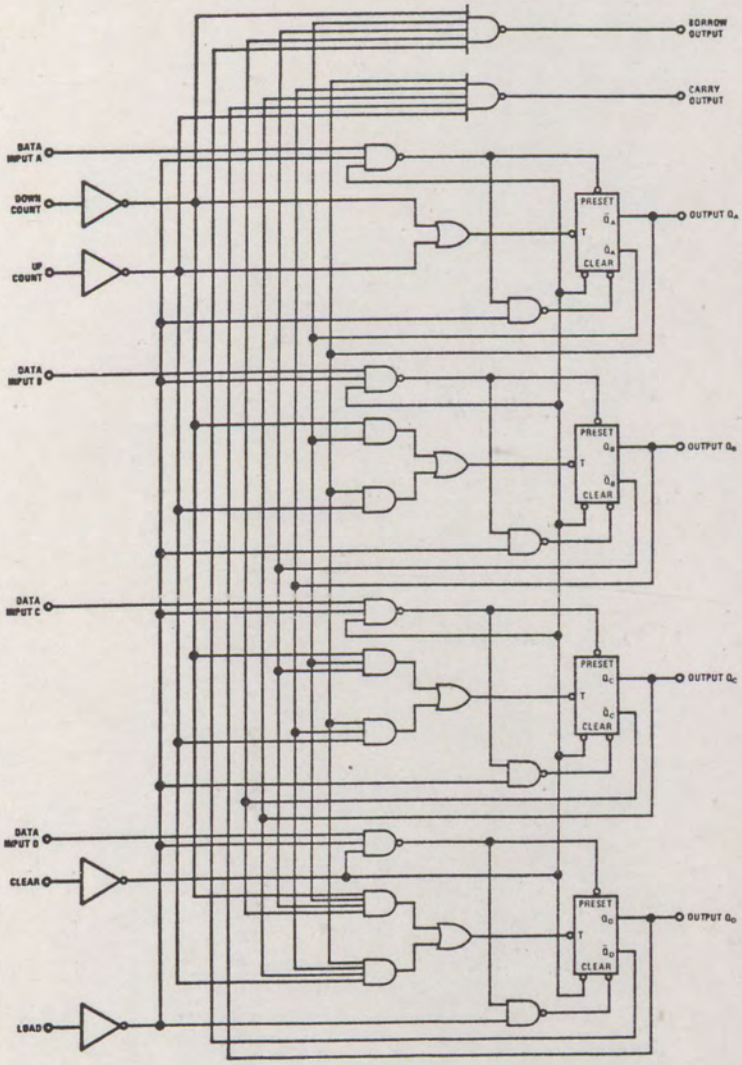
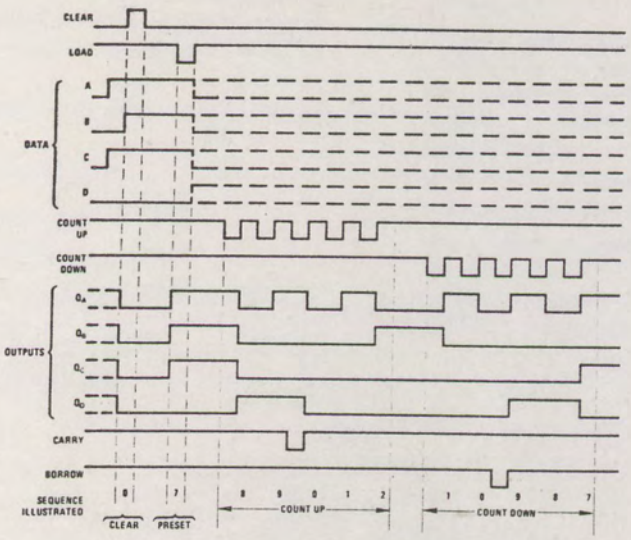
logic diagrams (cont.)

DM54L193/DM74L193



switching time waveforms

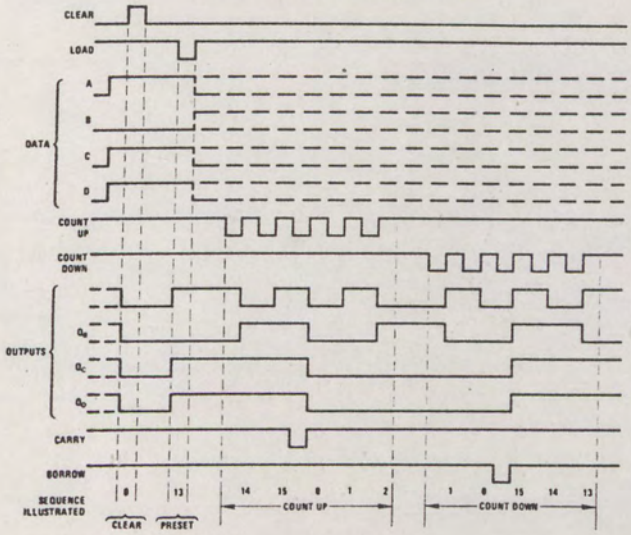
1. Clear outputs to zero.
2. Load (preset to BCD seven.
3. Count up to eight, nine, carry, zero, one and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



DM54L192/DM74L192

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



DM54L193/DM74L193

Operational Amplifiers

LM748/LM748C operational amplifier

general description

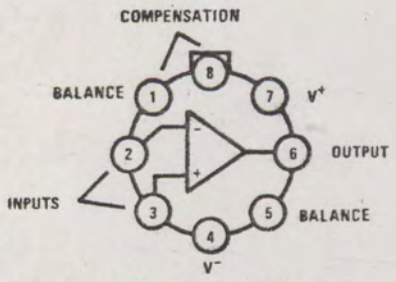
The LM748/LM748C is a general purpose operational amplifier built on a single silicon chip. The resulting close match and tight thermal coupling gives low offsets and temperature drift as well as fast recovery from thermal transients. In addition, the device features:

- Frequency compensation with a single 30 pF capacitor
- Operation from ±5V to ±20V
- Low current drain: 1.8 mA at ±20V
- Continuous short-circuit protection
- Operation as a comparator with differential inputs as high as ±30V
- No latch-up when common mode range is exceeded.
- Same pin configuration as the LM101.

The unity-gain compensation specified makes the circuit stable for all feedback configurations, even with capacitive loads. However, it is possible to optimize compensation for best high frequency performance at any gain. As a comparator, the output can be clamped at any desired level to make it compatible with logic circuits.

The LM748 is specified for operation over the −55°C to +125°C military temperature range. The LM748C is specified for operation over the 0°C to +70°C temperature range.

connection diagram

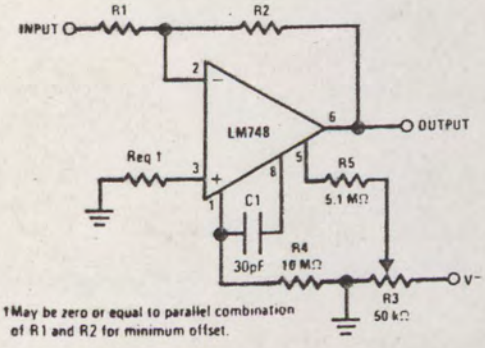


NOTE: Pin 4 connected to case.

Order Number LM748H or LM748CH
See Package 11

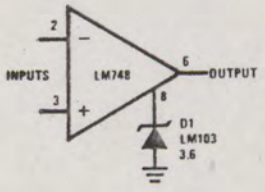
typical applications

Inverting Amplifier with Balancing Circuit

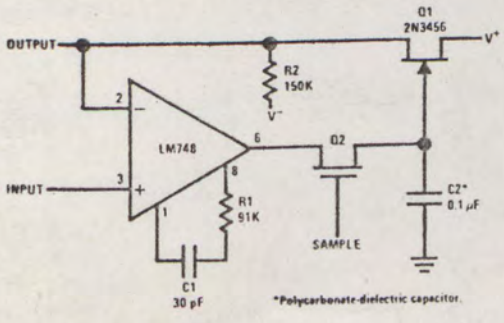


†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

Voltage Comparator for Driving DTL or TTL Integrated Circuits

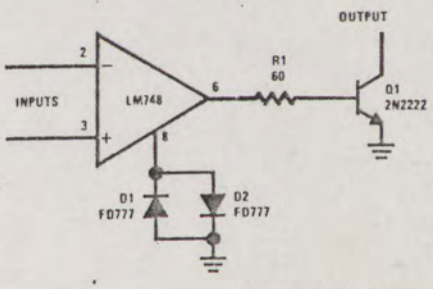


Low Drift Sample and Hold



*Polycarbonate-dielectric capacitor.

Voltage Comparator for Driving RTL Logic or High Current Driver



absolute maximum ratings

Supply Voltage	±22V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range: LM748	−55°C to +125°C
LM748C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
put Offset Voltage	$T_A = 25°C$, $R_S \leq 10\ k\Omega$		1.0	5.0	mV
put Offset Current	$T_A = 25°C$		40	200	nA
put Bias Current	$T_A = 25°C$		120	500	nA
put Resistance	$T_A = 25°C$	300	800		kΩ
pply Current	$T_A = 25°C$, $V_S = \pm 15V$		1.8	2.8	mA
arge Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	160		V/mV
put Offset Voltage	$R_S \leq 10\ k\Omega$			6.0	mV
verage Temperature Coefficient of Input Offset Voltage	$R_S \leq 50\Omega$		3.0		µV/°C
	$R_S \leq 10\ k\Omega$		6.0		µV/°C
nput Offset Current	$T_A = 0°C$ to $70°C$			300	nA
	$T_A = -55°C$ to $125°C$			500	nA
nput Bias Current	$T_A = 0°C$ to $70°C$			0.8	µA
	$T_A = -55°C$ to $125°C$			1.5	µA
Supply Current	$T_A = +125°C$, $V_S = \pm 15V$		1.2	2.25	mA
	$T_A = -55°C$ to $125°C$		1.9	3.3	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ K\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\Omega$	±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	90		dB

Note 1: For operating at elevated temperatures the devices must be derated based on a maximum junction to case thermal resistance of 45°C per watt, or 150°C per watt junction to ambient. (See Curves).

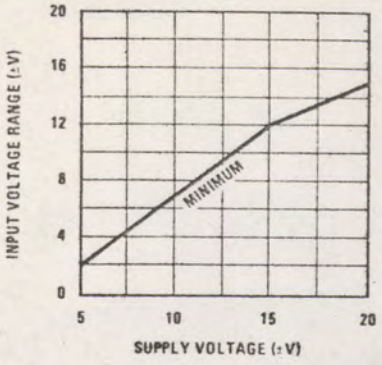
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to +125°C and ambient temperatures to +70°C.

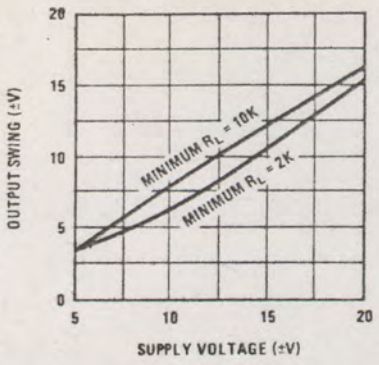
Note 4: These specifications apply for $\pm 5V \leq V_S \leq +15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM748C, however, all temperature specifications are limited to $0°C \leq T_A \leq 70°C$.

guaranteed performance characteristics (Note 4)

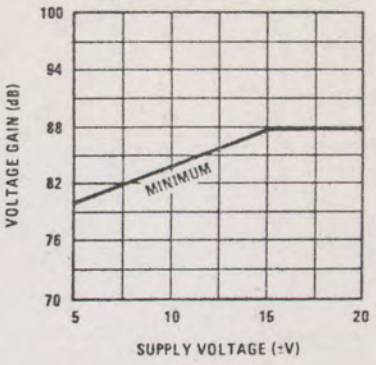
Input Voltage Range



Output Swing

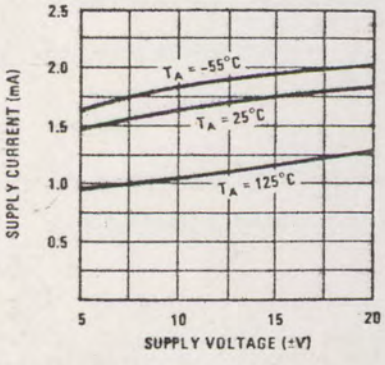


Voltage Gain

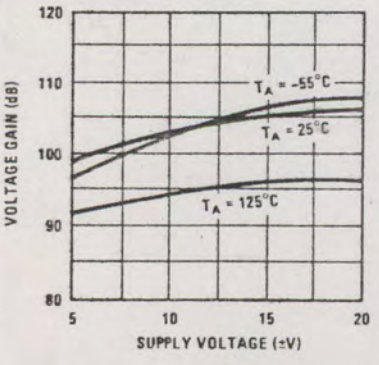


typical performance characteristics

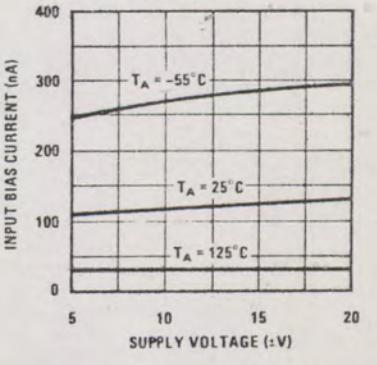
Supply Current



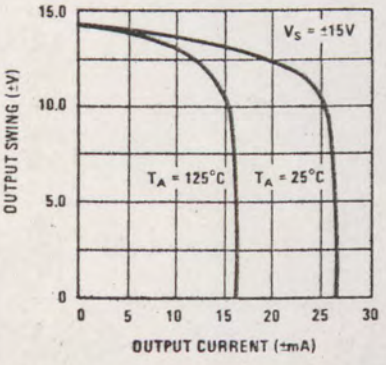
Voltage Gain



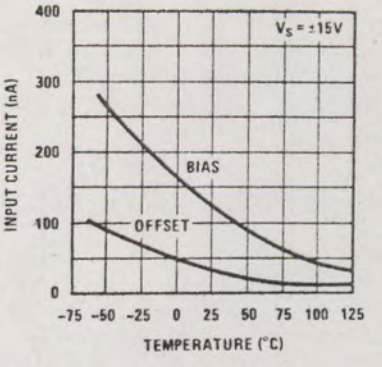
Input Bias Current



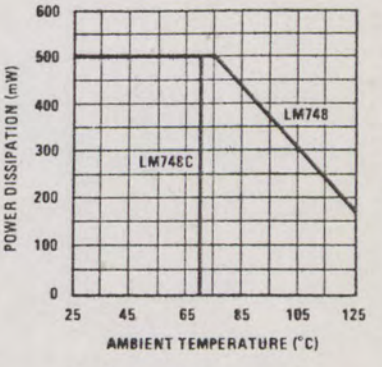
Current Limiting



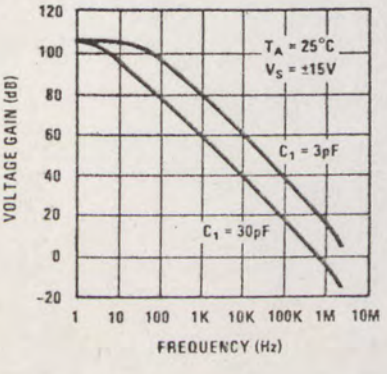
Input Current



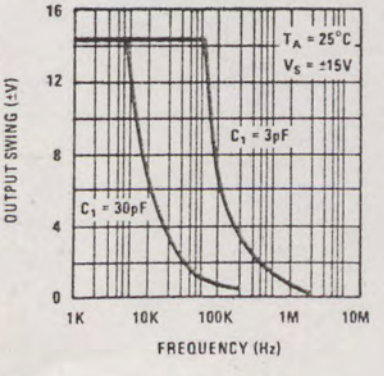
Maximum Power Dissipation



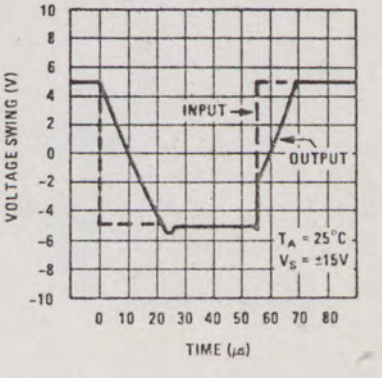
Open Loop
Frequency Response



Large Signal
Frequency Response



Voltage Follower
Pulse Response



Operational Amplifiers

241

LM1558/LM1458 dual operational amplifier

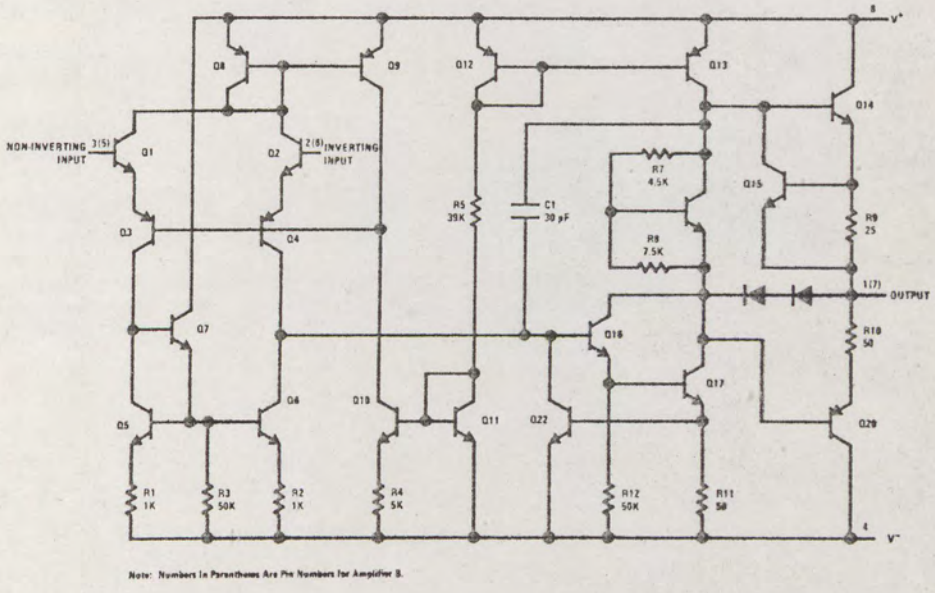
general description

The LM1558 and the LM1458 are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent. Features include:

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- 8-lead TO-5 and 8-lead mini DIP
- No latch up when input common mode range is exceeded

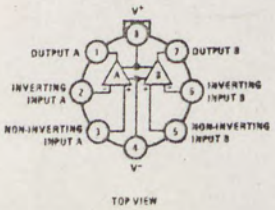
The LM1458 is identical to the LM1558 except that the LM1458 has its specifications guaranteed over the temperature range from 0°C to 70°C instead of −55°C to +125°C.

schematic and connection diagrams



Note: Numbers in Parentheses Are Pin Numbers for Amplifier B.

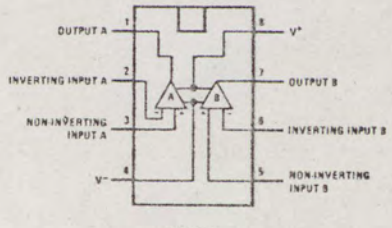
Metal Can Package



TOP VIEW

Order Number LM1458H or LM1558H
See Package 11

Dual-In-Line Package



TOP VIEW

Order Number LM1458N
See Package 20

absolute maximum ratings

Supply Voltage LM1558	±22V	Output Short-Circuit Duration	Indefinite
LM1458	±18V	Operating Temperature Range LM1558	−55°C to 125°C
Power Dissipation (Note 1) LM1558H/LM1458H	500 mW	LM1458	0°C to 70°C
LM1458N	400 mW	Storage Temperature Range	−65°C to 150°C
Differential Input Voltage	±30V	Lead Temperature (Soldering, 10 sec)	300°C
Input Voltage (Note 2)	±15V		

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	LM1558			LM1458			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10\ k\Omega$		1.0	5.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		80	200		80	200	nA
Input Bias Current	$T_A = 25°C$		200	500		200	500	nA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Supply Current Both Amplifiers	$T_A = 25°C$, $V_S = \pm 15V$		3.0	5.0		3.0	5.6	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	160		20	160		V/mV
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1.5			0.8	μA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	96		77	96		dB

Note 1: The maximum junction temperature of the LM1558 is 150°C, while that of the LM1458 is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 187°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM1458, however, all specifications are limited to $0°C \leq T_A \leq 70°C$ and $V_S = \pm 15V$.

Voltage Regulators

LM120 series three-terminal negative regulators

general description

The LM120 Series are three-terminal negative regulators with a fixed output voltage of −5V, −5.2V, −12V, and −15V and up to 1.5A load current capability. These devices need only one external component – a compensation capacitor at the output, making them easy to apply. Worst case guarantees on output voltage deviation due to any combination of line, load or temperature variation assure satisfactory system operation.

Exceptional effort has been made to make the LM120 Series immune to overload conditions. The regulators have current limiting which is independent of temperature, combined with thermal overload protection. Internal current limiting protects against momentary faults while thermal shutdown prevents junction temperatures from exceeding safe limits during prolonged overloads.

Although primarily intended for fixed output voltage applications, the LM120 Series may be programmed for higher output voltages with a simple resistive divider. The low quiescent drain current of the devices allows this technique to be used with good regulation.

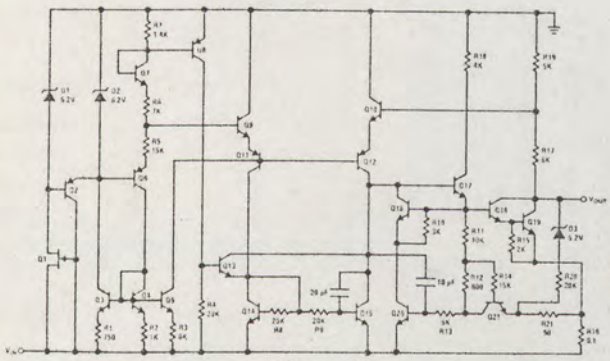
The LM120 Series is available in TO-5 and TO-3 packages. The TO-5 is rated at 200 mA and 2W; the TO-3 at 1A and 20W.

features

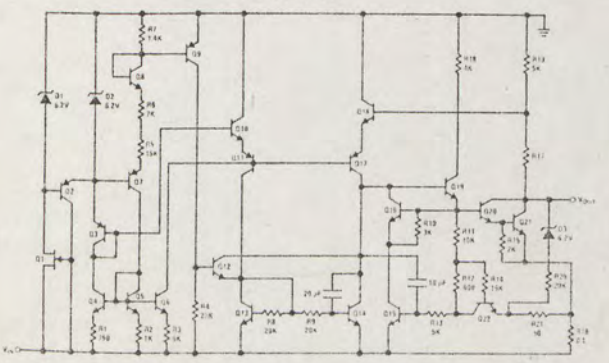
- Preset output voltage error less than ±3%
- Preset current limit
- Internal thermal shutdown
- Operates with input-output voltage differential down to 1V
- Excellent ripple rejection
- 50 mV load regulation

schematic and connection diagrams

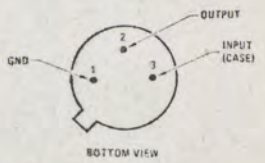
−5V & −5.2V



−12V & −15V



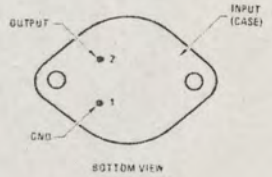
TO-5 (H)



BOTTOM VIEW

Order Numbers:
LM120H-05 LM120H-5.2 LM120H-12 LM120H-15
LM220H-05 LM220H-5.2 LM220H-12 LM220H-15
LM320H-05 LM320H-5.2 LM320H-12 LM320H-15
See Package 9

TO-3 (K)



BOTTOM VIEW

Order Numbers:
LM120K-05 LM120K-5.2 LM120K-12 LM120K-15
LM220K-05 LM220K-5.2 LM220K-12 LM220K-15
LM320K-05 LM320K-5.2 LM320K-12 LM320K-15
See Package 18

absolute maximum ratings

Device Type	Input Voltage	Input Output Differential
LM120 Series/ 5.0V	-25V	25V
LM120 Series/ 5.2V	-25V	25V
LM120 Series/ 12V	-35V	30V
LM120 Series/-15V	-40V	30V

Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LM120	-55°C to +150°C
LM220	-25°C to +150°C
LM320	0°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	300°C

electrical characteristics (-5V & -5.2V) (Note 1)

PARAMETER	CONDITIONS	LM120 LM220 MIN	LM120 LM220 MAX	TYP	LM320 MIN	LM320 MAX	UNITS
Output Voltage	$T_j = 25°C$ -5V	-5.1	-4.9	-5.0	-5.2	-4.8	V
	-5.2V	-5.3	-5.1	-5.2	-5.4	-5.0	V
Line Regulation (Note 2)	$T_j = 25°C$						
	$-25V \le V_{IN} \le -7V$		25	10		50	mV
Load Regulation (Note 2)	$T_j = 25°C$						
H Package	$5\ mA \le I_{OUT} \le 0.5A$		50	20		50	mV
K Package	$5\ mA \le I_{OUT} \le 1.5A$		75	50		100	mV
Output Voltage	$-25V \le V_{IN} \le -7V$						
	$5\ mA \le I_{OUT} \le I_{MAX}$						
	$P \le P_{MAX}$ -5V	-5.20	-4.80		-5.25	-4.75	V
	-5.2V	-5.40	-5.00		-5.45	-4.95	V
Quiescent Current	$-25V \le V_{IN} \le -7V$		2.0	1.0		2.0	mA
Quiescent Current Change	$T_A = 25°C$						
	$-25V \le V_{IN} \le -7V$		0.4	0.1		0.4	mA
	$5\ mA \le I_{OUT} \le I_{MAX}$		0.4	0.1		0.4	mA
Output Noise Voltage	$T_A = 25°C$, $C_L = 1\ \mu F$						
	$10\ Hz \le f \le 100\ kHz$			150			μV
Long Term Stability			50	5		50	mV
Thermal Resistance Junction to Case							
H Package				15			°C/W
K Package				3			°C/W

electrical characteristics (-12V) (Note 1)

PARAMETER	CONDITIONS	LM120 LM220 MIN	LM120 LM220 MAX	TYP	LM320 MIN	LM320 MAX	UNITS
Output Voltage	$T_j = 25°C$	-12.3	-11.7	-12	-12.4	-11.6	V
Line Regulation (Note 2)	$T_j = 25°C$						
	$-32V \le V_{IN} \le -14V$		10	4		20	mV
Load Regulation	$T_j = 25°C$						
H Package	$5\ mA \le I_{OUT} \le 0.2A$		25	10		40	mV
K Package (Note 2)	$5\ mA \le I_{OUT} \le 1.0A$		80	30		80	mV
Output Voltage	$-32V \le V_{IN} \le -14V$	-12.5	-11.5		-12.6	-11.4	V
	$5\ mA \le I_{OUT} \le I_{MAX}$						
	$P \le P_{MAX}$						
Quiescent Current	$-32V \le V_{IN} \le -14V$		4	2		4	mA
Quiescent Current Change	$T_j = 25°C$						
	$-32V \le V_{IN} \le -14V$			0.1			mA
	$5\ mA \le I_{OUT} \le I_{MAX}$			0.1			mA
Output Noise Voltage	$T_A = 25°C$			400			μV
	$10\ Hz < f \le 100\ kHz$						
Long Term Stability			120	15		120	mV

electrical characteristics (−15V) (Note 1)

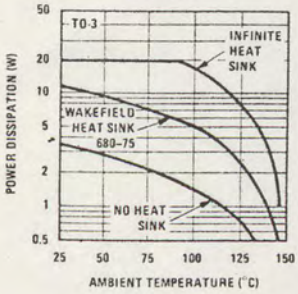
PARAMETER	CONDITIONS	LM120 LM220 MIN	LM120 LM220 MAX	TYP	LM320 MIN	LM320 MAX	UNITS
Output Voltage	$T_j = 25°C$	−15.3	−14.7	−15	−15.4	−14.6	V
Line Regulation (Note 2)	$T_j = 25°C$, $-35V \le V_{IN} \le -17V$		10	5		20	mV
Load Regulation (Note 2)	$T_j = 25°C$						
H Package	$5\ mA \le I_{OUT} \le 0.2A$		25	10		40	mV
K Package	$5\ mA \le I_{OUT} \le 1.0A$		80	30		80	mV
Output Voltage	$-35V \le V_{IN} \le -17V$, $5\ mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$	15.5	14.5		15.6	14.4	V
Quiescent Current	$-35V \le V_{IN} \le -17V$		4	2		4	mA
Quiescent Current Change	$T_j = 25°C$						
	$-35V \le V_{IN} \le -17V$			0.1			mA
	$5\ mA \le I_{OUT} \le I_{MAX}$			0.1			mA
Output Noise Voltage				400			μV
Long Term Stability			150	15		150	mV

Note 1: Unless otherwise specified, these specifications apply: $-55°C < T_j < 150°C$ for the LM120; $-25°C < T_j < 150°C$ for the LM220, and $0°C < T_j < 125°C$ for the LM320; $V_{IN} = (V_{OUT} + 5V)$ and $I_{OUT} = 0.1A$ for the TO-5 package and $I_{OUT} = 0.5A$ for the TO-3 package. For the TO-5 package, $I_{MAX} = 0.2A$ and $P_{MAX} = 2.0W$. For the TO-3 package, $I_{MAX} = 1.0A$ and $P_{MAX} = 20W$. Although power dissipation is internally limited, electrical specifications apply only for power levels up to P_{MAX}. For calculations of junction temperature rise due to power dissipation, use a thermal resistance of 150 °C/W for the TO-5 and 35 °C/W for the TO-3. With an infinite heat sink, the thermal resistance is 15 °C/W and 3 °C/W respectively.

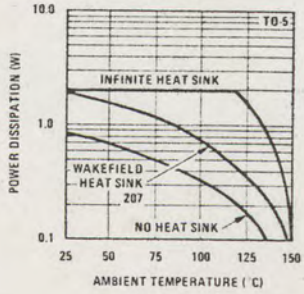
Note 2: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. To ensure constant junction temperature, pulse testing with a low duty cycle is used.

typical performance characteristics

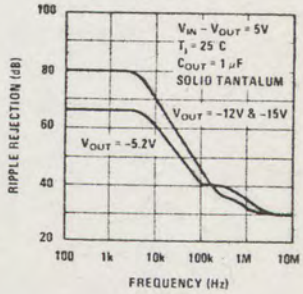
Maximum Average Power Dissipation



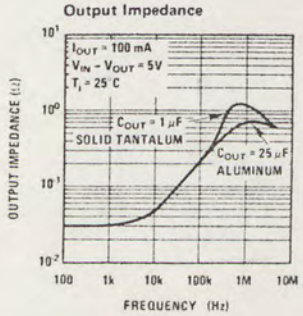
Maximum Average Power Dissipation



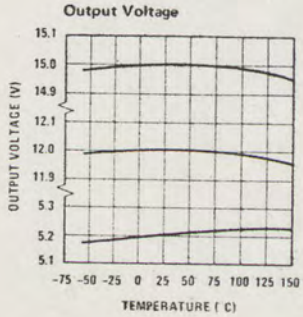
Ripple Rejection



Output Impedance



Output Voltage



Voltage Regulators

LM309 five-volt regulator

general description

The LM309 is a complete 5V regulator fabricated on a single silicon chip. It is designed for local regulation on digital logic cards, eliminating the distribution problems associated with single-point regulation. The device is available in two common transistor packages. In the solid-kovar TO-5 header, it can deliver output currents in excess of 200 mA, if adequate heat sinking is provided. With the TO-3 power package, the available output current is greater than 1A.

The regulator is essentially blow-out proof. Current limiting is included to limit the peak output current to a safe value. In addition, thermal shutdown is provided to keep the IC from overheating. If internal dissipation becomes too great, the regulator will shut down to prevent excessive heating.

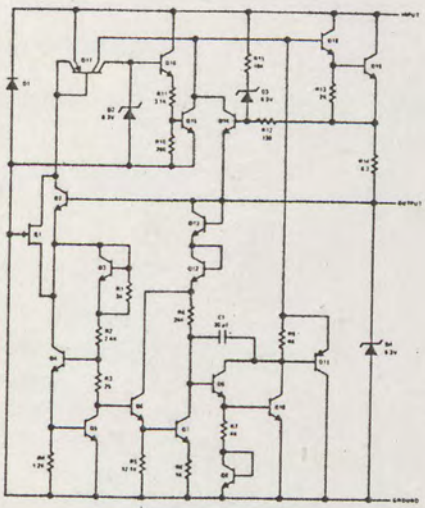
Considerable effort was expended to make the LM309 easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response somewhat. Input bypassing is needed, however, if the regulator is located very far from the filter capacitor of the power supply. Stability is also achieved by methods that provide very good rejection of load or line transients as are usually seen with TTL logic.

Although designed primarily as a fixed-voltage regulator, the output of the LM309 can be set to voltages above 5V, as shown below. It is also possible to use the circuit as the control element in precision regulators, taking advantage of the good current-handling capability and the thermal overload protection.

To summarize, outstanding features of the regulator are:

- Specified to be compatible, worst case, with TTL and DTL
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required

schematic diagram

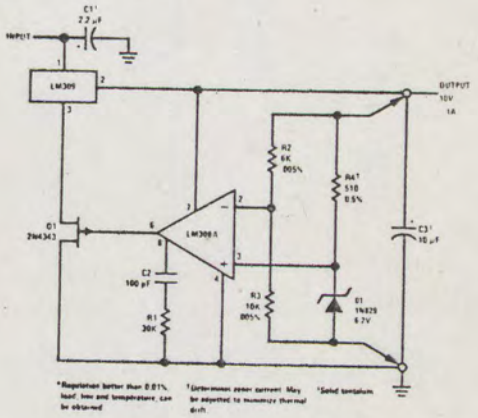


Order Number LM309H
See Package 9

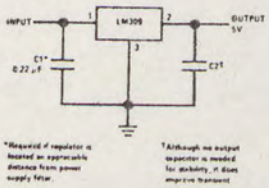
Order Number LM309K
See Package 18

typical applications

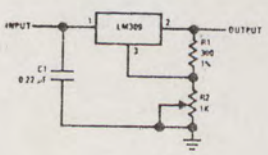
High Stability Regulator*



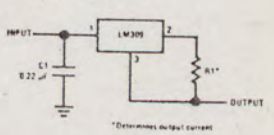
Fixed 5V Regulator



Adjustable Output Regulator



Current Regulator



absolute maximum ratings

Input Voltage	35V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	0°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

design characteristics (Note 1)

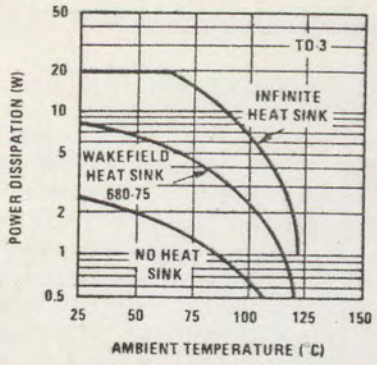
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_j = 25°C$	4.8	5.05	5.2	V
Line Regulation	$T_j = 25°C$				
	$7V \leq V_{IN} \leq 25V$		4.0	50	mV
Load Regulation	$T_j = 25°C$				
LM309H	$5\ mA \leq I_{OUT} \leq 0.5A$		20	50	mV
LM309K	$5\ mA \leq I_{OUT} \leq 1.5A$		50	100	mV
Output Voltage	$7V \leq V_{IN} \leq 25V$				
	$5\ mA \leq I_{OUT} \leq I_{max}$ $P < P_{max}$	4.75		5.25	V
Quiescent Current	$7V \leq V_{IN} \leq 25V$		5.2	10	mA
Quiescent Current Change	$7V \leq V_{IN} \leq 25V$			0.5	mA
	$5\ mA \leq I_{OUT} \leq I_{max}$			0.8	mA
Output Noise Voltage	$T_A = 25°C$				
	$10\ Hz \leq f \leq 100\ kHz$		40		μV
Long Term Stability				20	mV
Thermal Resistance					
Junction to Case (Note 2)					
LM309H			15		°C/W
LM309K			3.0		°C/W

Note 1: Unless otherwise specified, these specifications apply for $0°C \leq T_j \leq 125°C$, $V_{IN} = 10V$ and $I_{OUT} = 0.1A$ for the LM309H or $I_{OUT} = 0.5A$ for the LM309K. For the LM309H, $I_{max} = 0.2A$ and $P_{max} = 2.0W$. For the LM309K, $I_{max} = 1.0A$ and $P_{max} = 20W$.

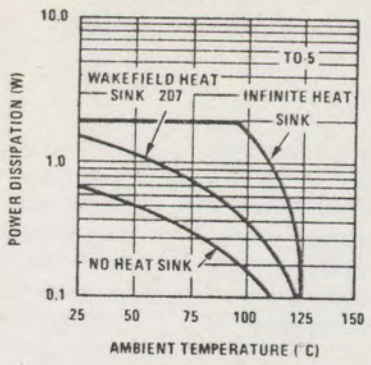
Note 2: Without a heat sink, the thermal resistance of the TO-5 package is about 150°C/W, while that of the TO-3 package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

typical performance characteristics

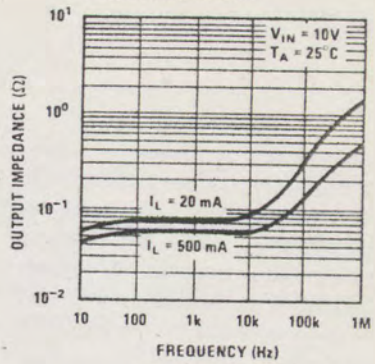
Maximum Average Power Dissipation



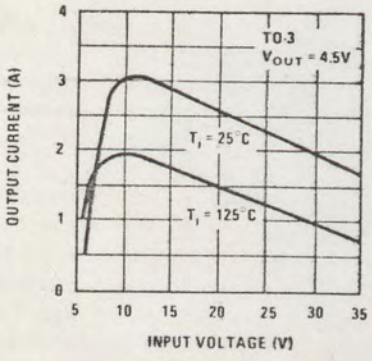
Maximum Average Power Dissipation



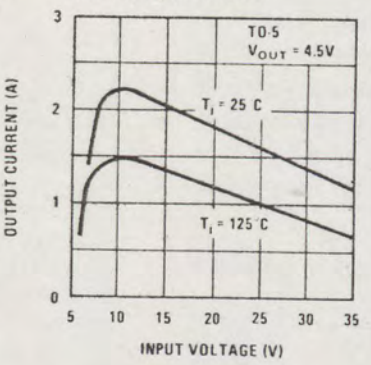
Output Impedance



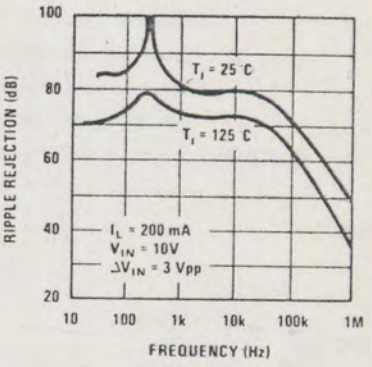
Peak Output Current



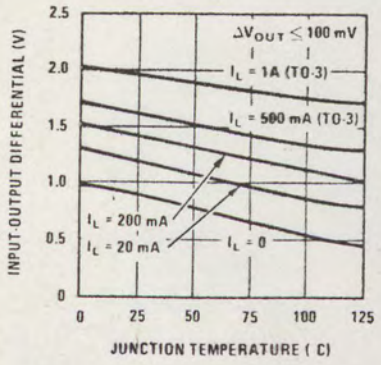
Peak Output Current



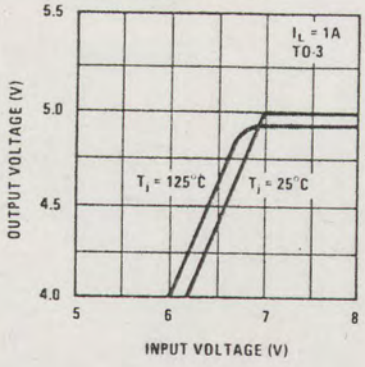
Ripple Rejection



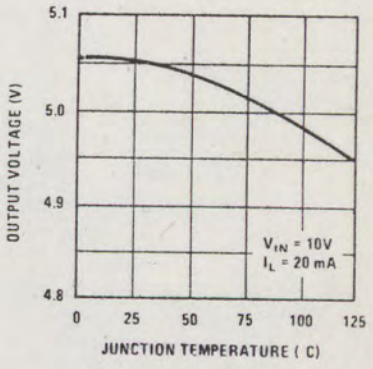
Dropout Voltage



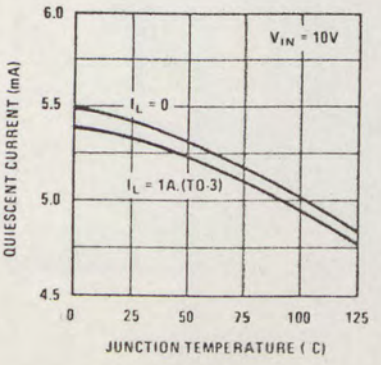
Dropout Characteristic



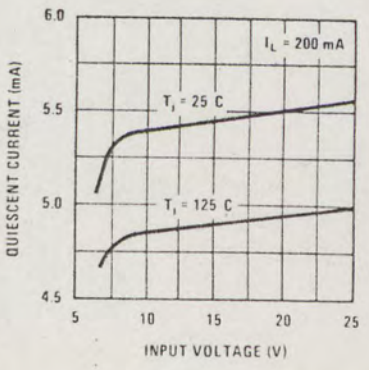
Output Voltage



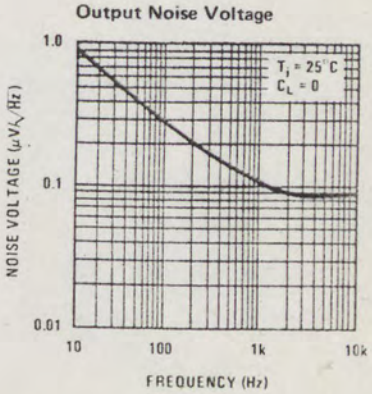
Quiescent Current



Quiescent Current



Output Noise Voltage



Voltage Regulators

LM340 series voltage regulators

general description

The LM340-XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM340-XX series is available in two power packages. Both the plastic TO-220 and metal TO-3 packages allow these regulators to deliver over 1.0A if adequate heat sinking is provided. Even with over 1.0A of output current available the regulators are essentially blow-out proof. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM340-XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

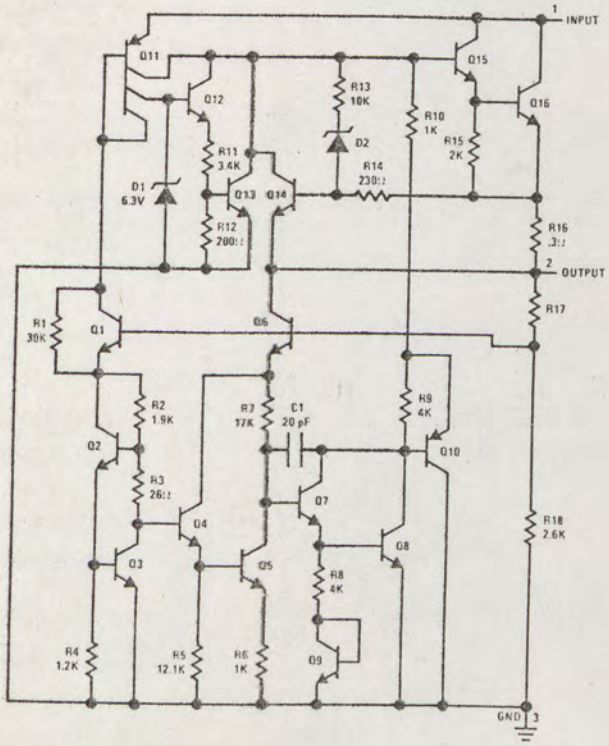
features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-220 and metal TO-3 packages

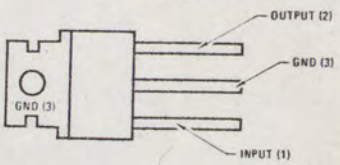
voltage range

LM340-05	5V	LM340-15	15V
LM340-06	6V	LM340-18	18V
LM340-08	8V	LM340-24	24V
LM340-12	12V		

schematic and connection diagrams



TO-220 (T)



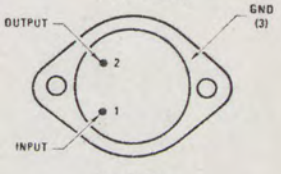
TOP VIEW

Order Numbers:

LM340-05T LM340-15T
LM340-06T LM340-18T
LM340-08T LM340-24T
LM340-12T

See Package 26

TO-3 (K)



BOTTOM VIEW

Order Numbers:

LM340-05K LM340-15K
LM340-06K LM340-18K
LM340-08K LM340-24K
LM340-12K

See Package 18

absolute maximum ratings

Input Voltage (V_O = 5V through 18V)	35V
(V_O = 24V)	40V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	0°C to 70°C
Maximum Junction Temperature	
TO-3 Package	150°C
TO-220 Package	125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature	
To-3 Package (Soldering, 10 sec)	300°C
TO-220 Package (Soldering, 10 sec)	230°C

electrical characteristics

LM340-05 (V_{IN} = 10V, I_{OUT} = 500 mA, 0°C ≤ T_A ≤ 70°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	T_j = 25°C	4.8	5.0	5.2	V
Line Regulation	T_j = 25°C, 7V ≤ V_{IN} ≤ 25V				
	I_{OUT} = 100 mA			50	mV
	I_{OUT} = 500 mA			100	mV
Load Regulation	T_j = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5A			100	mV
Output Voltage	7V ≤ V_{IN} ≤ 20V, 5 mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W	4.75		5.25	V
Quiescent Current	T_j = 25°C		6.0	10	mA
Quiescent Current Change	7V ≤ V_{IN} ≤ 25V			1.3	mA
	5 mA ≤ I_{OUT} ≤ 1.5A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		40		μV
Long Term Stability				20	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		70		dB
Dropout Voltage	T_j = 25°C, I_{OUT} = 1.0A		2.0		V

LM340-06 (V_{IN} = 11V, I_{OUT} = 500 mA, 0°C ≤ T_A ≤ 70°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	T_j = 25°C	5.75	6.0	6.25	V
Line Regulation	T_j = 25°C, 8V ≤ V_{IN} ≤ 25V				
	I_{OUT} = 100 mA			60	mV
	I_{OUT} = 500 mA			120	mV
Load Regulation	T_j = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5A			120	mV
Output Voltage	8V ≤ V_{IN} ≤ 21V, 5 mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W	5.7		6.3	V
Quiescent Current	T_j = 25°C		6.0	10	mA
Quiescent Current Change	8V ≤ V_{IN} ≤ 25V			1.3	mA
	5 mA ≤ I_{OUT} ≤ 1.5A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		45		μV
Long Term Stability				24	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		65		dB
Dropout Voltage	T_j = 25°C, I_{OUT} = 1.0A		2.0		V

Note 1: Thermal resistance without a heat sink for junction to case temperature is 4.0°C/W for the TO-3 package and 2.0°C/W for the TO-220 package. Thermal resistance for case to ambient temperature is 35°C/W for the TO-3 package and 50°C/W for the TO-220 package.

electrical characteristics (con't)

LM340-08 (V_{IN} = 14V, I_{OUT} = 500 mA, $0°C \leq T_A \leq 70°C$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_j = 25°C$	7.7	8.0	8.3	V
Line Regulation	$T_j = 25°C$, $10.5V \leq V_{IN} \leq 25V$				
	I_{OUT} = 100 mA			80	mV
	I_{OUT} = 500 mA			160	mV
Load Regulation	$T_j = 25°C$, 5 mA $\leq I_{OUT} \leq$ 1.5A			160	mV
Output Voltage	$10.5V \leq V_{IN} \leq 23V$, 5 mA $\leq I_{OUT} \leq$ 1.0A, $P_D \leq$ 15W	7.6		8.4	V
Quiescent Current	$T_j = 25°C$		6.0	10	mA
Quiescent Current Change	$10.5V \leq V_{IN} \leq 25V$			1.0	mA
	5 mA $\leq I_{OUT} \leq$ 1.5A			0.5	mA
Output Noise Voltage	$T_A = 25°C$, 10 Hz $\leq f \leq$ 100 kHz		52		μV
Long Term Stability				32	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		62		dB
Dropout Voltage	$T_j = 25°C$, I_{OUT} = 1.0A		2.0		V

LM340-12 (V_{IN} = 19V, I_{OUT} = 500 mA, $0°C \leq T_A \leq 70°C$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_j = 25°C$	11.5	12.0	12.5	V
Line Regulation	$T_j = 25°C$, $14.5V \leq V_{IN} \leq 30V$				
	I_{OUT} = 100 mA			120	mV
	I_{OUT} = 500 mA			240	mV
Load Regulation	$T_j = 25°C$, 5 mA $\leq I_{OUT} \leq$ 1.5A			240	mV
Output Voltage	$14.5V \leq V_{IN} \leq 27V$, 5 mA $\leq I_{OUT} \leq$ 1.0A, $P_D \leq$ 15W	11.4		12.6	V
Quiescent Current	$T_j = 25°C$		6.0	10	mA
Quiescent Current Change	$14.5V \leq V_{IN} \leq 30V$			1.0	mA
	5 mA $\leq I_{OUT} \leq$ 1.5A			0.5	mA
Output Noise Voltage	$T_A = 25°C$, 10 Hz $\leq f \leq$ 100 kHz		75		μV
Long Term Stability				48	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		61		dB
Dropout Voltage	$T_j = 25°C$, I_{OUT} = 1.0A		2.0		V

LM340-15 (V_{IN} = 23V, I_{OUT} = 500 mA, $0°C \leq T_A \leq 70°C$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_j = 25°C$	14.4	15.0	15.6	V
Line Regulation	$T_j = 25°C$, $17.5V \leq V_{IN} \leq 30V$				
	I_{OUT} = 100 mA			150	mV
	I_{OUT} = 500 mA			300	mV
Load Regulation	$T_j = 25°C$, 5 mA $\leq I_{OUT} \leq$ 1.5A			300	mV
Output Voltage	$17.5V \leq V_{IN} \leq 30V$, 5 mA $\leq I_{OUT} \leq$ 1.0A, $P_D \leq$ 15W	14.25		15.75	V
Quiescent Current	$T_j = 25°C$		6.0	10	mA
Quiescent Current Change	$17.5V \leq V_{IN} \leq 30V$			1.0	mA
	5 mA $\leq I_{OUT} \leq$ 1.5A			0.5	mA
Output Noise Voltage	$T_A = 25°C$, 10 Hz $\leq f \leq$ 100 kHz		90		μV
Long Term Stability				60	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		60		dB
Dropout Voltage	$T_j = 25°C$, I_{OUT} = 1.0A		2.0		V

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electrical characteristics (con't)

LM340-18 (V_{IN} = 27V, I_{OUT} = 500 mA, 0°C ≤ T_A ≤ 70°C, unless otherwise specified)

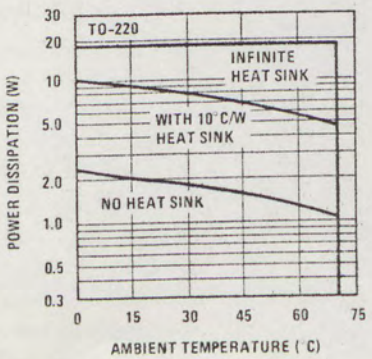
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	T_j = 25°C	17.3	18.0	18.7	V
Line Regulation	T_j = 25°C, 21V ≤ V_{IN} ≤ 33V				
	I_{OUT} = 100 mA			180	mV
	I_{OUT} = 500 mA			360	mV
Load Regulation	T_j = 25°C, 5 mA ≤ I_{OUT} ≤ 1.0A			360	mV
Output Voltage	21V ≤ V_{IN} ≤ 33V, 5 mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W	17.1		18.9	V
Quiescent Current	T_j = 25°C		6.0	10	mA
Quiescent Current Change	21V ≤ V_{IN} ≤ 33V			1.0	mA
	5 mA ≤ I_{OUT} ≤ 1.0A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		110		μV
Long Term Stability				72	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		59		dB
Dropout Voltage	T_j = 25°C, I_{OUT} = 1.0A		2.0		V

LM340-24 (V_{IN} = 33V, I_{OUT} = 500 mA, 0°C ≤ T_A ≤ 70°C, unless otherwise specified)

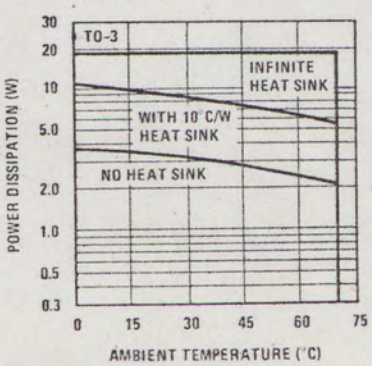
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	T_j = 25°C	23.0	24.0	25.0	V
Line Regulation	T_j = 25°C, 27V ≤ V_{IN} ≤ 38V				
	I_{OUT} = 100 mA			240	mV
	I_{OUT} = 500 mA			480	mV
Load Regulation	T_j = 25°C, 5 mA ≤ I_{OUT} ≤ 1.0A			480	mV
Output Voltage	27V ≤ V_{IN} ≤ 38V, 5 mA ≤ I_{OUT} ≤ 1.0A, P_D ≤ 15W	22.8		25.2	V
Quiescent Current	T_j = 25°C		6.0	10	mA
Quiescent Current Change	27V ≤ V_{IN} ≤ 38V			1.0	mA
	5 mA ≤ I_{OUT} ≤ 1.0A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		170		μV
Long Term Stability				96	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		56		dB
Dropout Voltage	T_j = 25°C, I_{OUT} = 1.0A		2.0		V

typical performance characteristics

Maximum Average Power Dissipation



Maximum Average Power Dissipation



DATEL SYSTEMS, INC.

FAST, 8 BIT ANALOG TO DIGITAL CONVERTER

MODEL ADC-EH8B

FEATURES

- 8 Bit Resolution
- 4.0 & 2.4 μsec. Conversion Time
- Unipolar or Bipolar Operation
- Parallel & Serial Outputs
- Low Cost

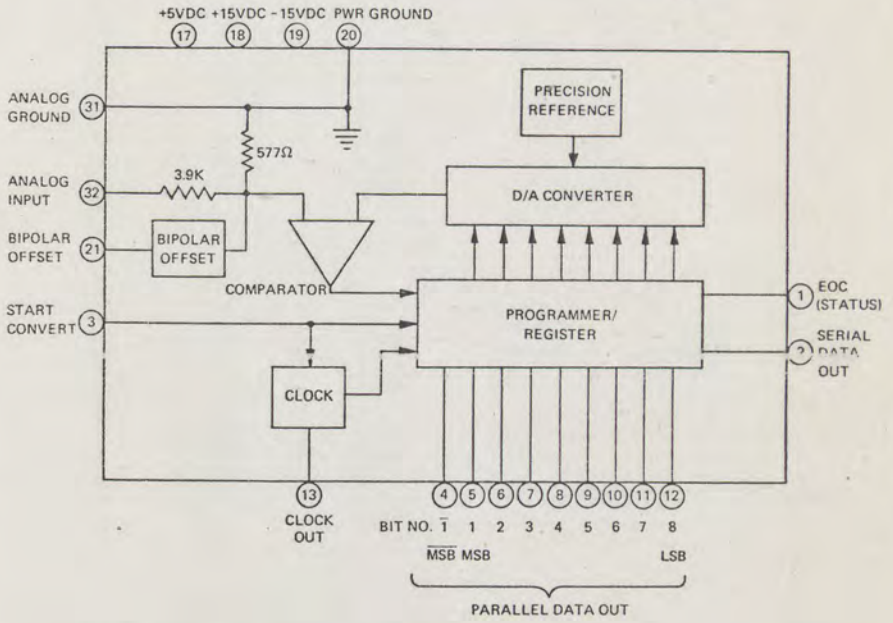
GENERAL DESCRIPTION

The model ADC-EH8B is a fast, 8 bit successive approximation type analog to digital converter in a compact 2 x 2 x .375 inch module. These converters are low cost devices with application in pulse code modulation systems and instrumentation and control systems requiring fast data conversion rates up to 400,000 per second. There are two models to choose from based on conversion speed: ADC-EH8B1 with a conversion time of 4.0 μsec. (250 kHz rate), and ADC-EH8B2 with a conversion time of 2.4 μsec. (416 kHz rate).

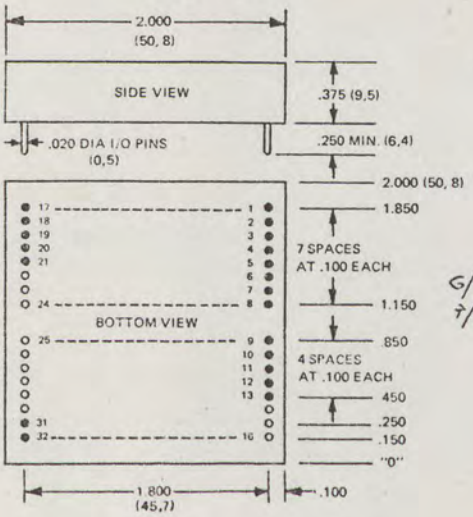
The high speed in a small size is made possible by the use of an MSI integrated circuit which provides all the necessary successive approximation logic, along with other new integrated circuit components. The analog input range is either unipolar 0 to +10V or bipolar −5V to +5V, determined by external pin connection. For unipolar operation no external adjustments are necessary; for bipolar operation only a bipolar offset adjustment must be made externally. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. A serial output gives successive decision pulses in NRZ format with straight or offset binary coding. Other outputs are clock output for synchronization with serial data, and $\overline{\text{MSB}}$ output for two's complement coding.

Other specifications include full scale temperature coefficient of 50 ppm/°C max., long term stability of .05%/year, and linearity of ±1/2 LSB. Power requirement is ±15VDC and +5VDC.

The ADC-EH8B1 & 2 are improved versions of Datel's former models ADC-EH1 & 2, and are identical in all specifications and pin positions except for a small change in input impedance and three added output pins for Clock Out, $\overline{\text{MSB}}$ Out, and Serial Data Out.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	SERIAL DATA OUTPUT
3	START CONVERT
4	BIT 1 OUT ($\overline{\text{MSB}}$)
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT
11	BIT 7 OUT
12	BIT 8 OUT (LSB)
13	CLOCK OUT
17	+5V POWER IN
18	+15V POWER IN
19	−15V POWER IN
20	POWER GROUND
21	BIPOLAR OFFSET
31	ANALOG GROUND
32	ANALOG INPUT

NOTES

1. Open dots designate omitted pins.
2. 0.100 inch = 2.5 mm, 0.150 inch = 3.8 mm.

I ? E.O.C. SBZ

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CIFICATIONS, ADC-EH8B

cal @ 25°C, +15V & +5V Supply, unless otherwise noted)

TS

g Input Range	0V to +10V FS or ±5V FS
Impedance	4.45K ohms ±50 ohms
Overvoltage	±20V (no damage)
Conversion	2V min. to 5.5V max. positive pulse with duration of 100 nsec. min. Rise and fall times <500 ns. Logic "1" resets converter Logic "0" initiates conversion Loading: 1 TTL load

UTS

l Output Data	8 parallel lines of data held until next conversion command. V out ("0") ≤ +0.4V V out ("1") ≥ +2.4V Each output capable of driving up to 4 TTL loads.
, Unipolar Operation	Straight Binary, positive true
Bipolar Operation	Offset Binary, positive true. Two's Complement, positive true.
Output Data	NRZ successive decision pulse output generated during conversion, with MSB first. Straight binary or offset binary coding. Loading: 4 TTL loads
Conversion (EOC)	Conversion Status Signal. V out ("0") ≤ +0.8V indicates conversion time completed. V out ("1") ≥ +2.4V during reset and conversion periods. Loading: 4 TTL loads.
Output	Internal clock pulse train of negative going pulses from +5V to 0V gated on during conversion time. Loading: 6 TTL loads

RMANCE

tion	8 Bits (1 part in 256)
cy at 25°C	±0.2% of FS ± 1/2 LSB
ty	± 1/2 LSB
ntial Nonlinearity	±1/2 LSB max.
Coeff. of Gain	± 50ppm/°C max.
Coeff. of Zero, Unipolar	± 100μV/°C max.
Coeff. of Offset, Bipolar	± 35 ppm of FS/°C max.
erm Stability	± .05%/year
Supply Rejection	± .02% of FS/% supply, max.
sion Time	4.0 μsec. max., ADC-EH8B1 2.4 μsec. max., ADC-EH8B2

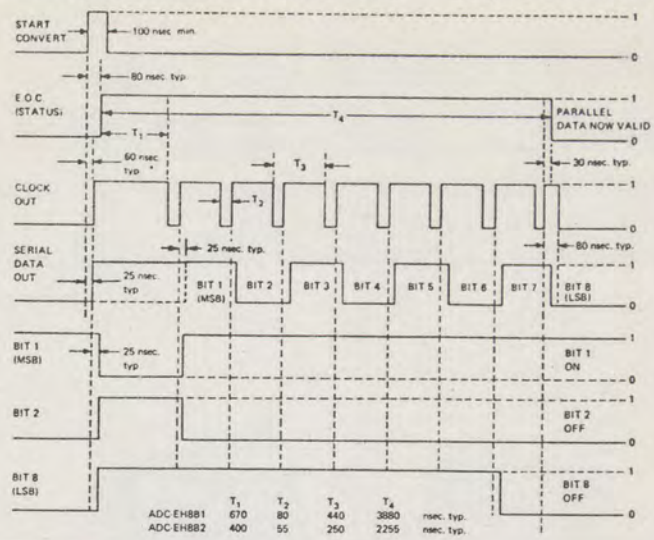
REQUIREMENT

± 15VDC ±0.5V @ 25mA max.
+5VDC ± 0.25V @ 125mA max.

CAL-ENVIRONMENTAL

ng Temp. Range	0°C to 70°C
Temp. Range	−55°C to +85°C
e Humidity	Up to 100% non-condensing
e	2 x 2 x 0.375 inches (50,8 x 50,8 x 9,5 mm)
terial	Black diallyl phthalate per MIL-M-14
	.020" round, gold plated, .250" lg. min.
	2 oz. max. (57g.)

TIMING DIAGRAM FOR ADC-EH8B Output: 10101010



OUTPUT CODING

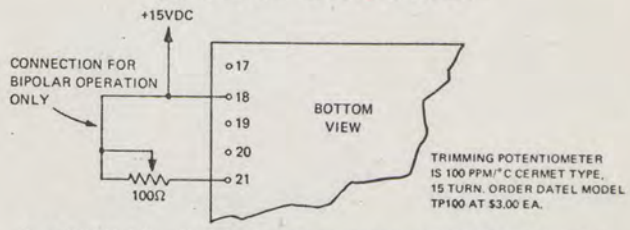
UNIPOLAR (0 TO +10V)

SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS−1 LSB	+9.96V	1111 1111
+7/8 FS	+8.75V	1110 0000
+3/4 FS	+7.50V	1100 0000
+1/2 FS	+5.00V	1000 0000
+1/4 FS	+2.50V	0100 0000
+1 LSB	+0.04V	0000 0001
0	0.00V	0000 0000

BIPOLAR (−5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BIN	2'S COMPLEMENT
+FS−1 LSB	+4.96V	1111 1111	0111 1111
+3/4 FS	+3.75V	1110 0000	0110 0000
+1/2 FS	+2.50V	1100 0000	0100 0000
0	0.00V	1000 0000	0000 0000
−1/2 FS	−2.50V	0100 0000	1100 0000
−3/4 FS	−3.75V	0010 0000	1010 0000
−FS+1 LSB	−4.96V	0000 0001	1000 0001
−FS	−5.00V	0000 0000	1000 0000

ADC-EH8B CALIBRATION



1. UNIPOLAR – No adjustments are necessary and 100Ω trimming pot is not used. Full scale and zero are internally set to better than 1/2 LSB. Pin 21 is left open.
2. BIPOLAR – Connect pin 18 (+15VDC) to pin 21 through a 100Ω trimming potentiometer as shown. Connect a precision voltage source to pin 32 and set the input voltage to + 1/2 LSB or +0.020V. Adjust the trimming potentiometer so that the output code flickers equally between 1000 0000 and 1000 0001.

ORDERING INFORMATION

DC-EH8B ____

NVERSION TIME
1 = 4.0 μSEC.
2 = 2.4 μSEC.

PRICES (1-9)

ADC-EH8B1	$ 85.00
ADC-EH8B2	$129.00

MATING SOCKETS:

DILS-2 (2/MODULE)	$5.00/PAIR
TP100 TRIMMING POT.	$3.00 EA.

For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing.

−EX	−25°C to +85°C operation
−EXX−HS	−55°C to +85°C operation with hermetically sealed semiconductor components.

NOTE: ADC-EH8B1 & 2 replace former models ADC-EH1 & 2 and are improved models of these units respectively. The only difference from the previous models is the 3 additional output pins for serial output, clock output, and $\overline{MSB}$ output, and a change in input impedance from 5K ohms to 4.45K ohms. If the newly used pins (nos. 2, 4, and 13) cause a problem in an existing application, they should be clipped off.

ATEL
STEMS, INC. 1020 TURNPIKE STREET, CANTON, MASS. 02021 TEL. (617) 828-8000 (714) 835-2751 (408) 733-2424 TWX: 710-348-0135 TELEX: 924461

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

11/75 Bulletin AEHDL10511

ANALOG DEVICES

Low Cost General Purpose Digital to Analog Converter

DAC-10Z/MDA-10Z

FEATURES
- Low Cost: $27 (100+)
- 10 Bit Resolution
- ±½LSB Linearity Error
- Unipolar or Bipolar Outputs
- Small Size (2" x 2" x 0.4")

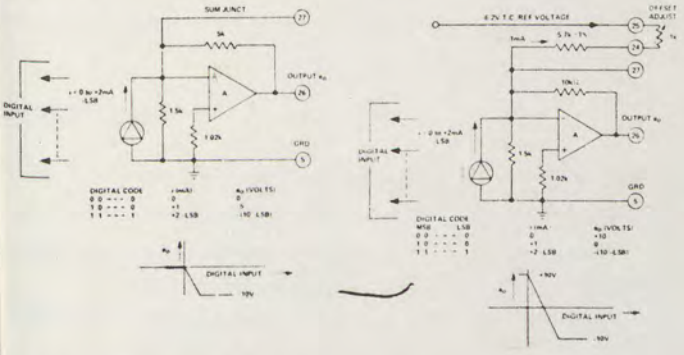
GENERAL DESCRIPTION

The MDA-10Z and DAC-10Z are low cost, 10-bit digital-to-analog converters packaged in compact 2" x 2" x 0.4" modules. The MDA-10Z is a current output device intended for use with external output amplifiers. It features a settling time to ±½LSB of 300ns. The DAC-10Z which comes complete with an IC op amp produces voltage outputs with 5μs settling times.

Both the DAC-10Z and MDA-10Z can be ordered with either unipolar or bipolar outputs. Unipolar units utilize Binary coded inputs and bipolar units use Offset Binary code. All digital inputs are fully TTL/DTL compatible.

DAC-10Z OUTPUT CHARACTERISTICS

The output circuit configuration as well as the input-output relationships of the DAC-10Z are shown below in Figure 1 for both the unipolar and bipolar output versions.



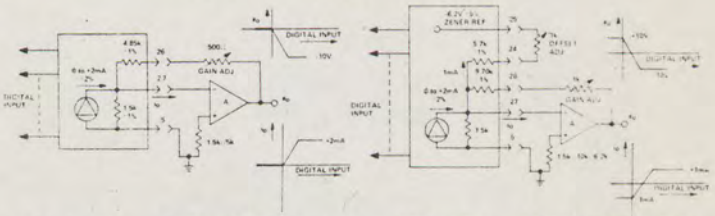
a) Unipolar – DAC-10Z-1 *b) Bipolar – DAC-10Z-3*

Figure 1. DAC-10Z Output Configuration

Note that the DAC-10Z-1 requires no external gain or zero adjustment. The DAC-10Z-3 requires a 1kΩ offset adjustment pot, which the user must supply. With a digital input of 0000000000 applied, this pot is adjusted until an output of +10.000V is obtained within ±2mV.

MDA-10Z WITH EXTERNAL AMPLIFIER

Figure 2, below, shows unipolar and bipolar versions of the MDA-10Z used with an external inverting op amp and also shows the resulting input-output relationships.



a) Unipolar – MDA-10Z-25 *b) Bipolar – MDA-10Z-110*

Figure 2. MDA-10Z With External Amplifier (Inverting Mode)

The gain of the MDA-10Z-25 is adjusted by means of a 500Ω trim pot which the user supplies. With a digital input of 1111111111 applied, this pot is adjusted until an output of –9.990V is obtained within ±1mV.

In addition to the gain adjustment, the MDA-10Z-110 requires a zero adjustment. With a digital input of 0000000000 applied, the 1kΩ offset pot is adjusted until a +10.000V output is obtained within ±2mV. Next, a digital input of 1111111111 is applied and the 1kΩ gain pot is adjusted until an output of –9.980V results within ±2mV.

Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast Tel: 213/595-1783
Mid-West Tel: 312/297-8710

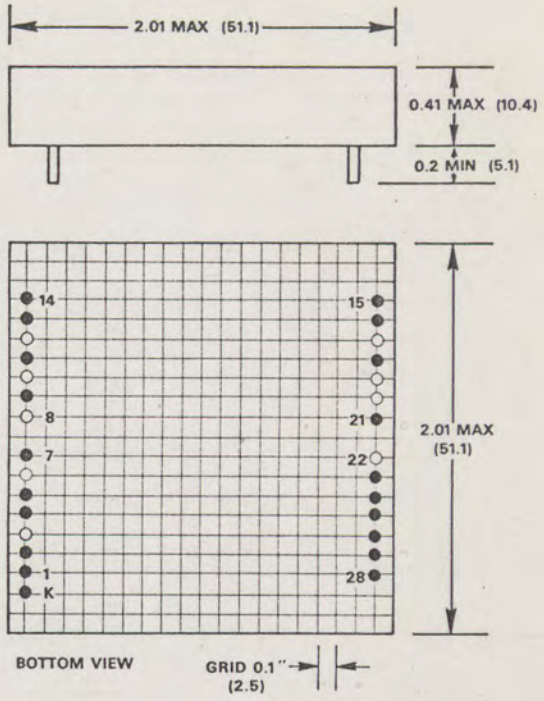
SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

MODELS	DAC-10Z	MDA-10Z
RESOLUTION	10 Bits Binary	•
DATA INPUTS		
0V ≤ "0" ≤ +0.8V[1]	-1.2mA	•
2.4V ≤ "1" ≤ +5V (For Open Circuit)	+25nA	•
CODING		
Unipolar Output	Natural Binary	•
Bipolar Output	Offset Binary	•
OUTPUT		
UNIPOLAR		
Voltage	0V to -10V	See Terminal Limits
Current	See Terminal Limits	0mA to +2mA
Zero Offset	¼LSB (2.5mV) Max	1/40LSB (50nA) Max
BIPOLAR		
Voltage	±10V	See Terminal Limits
Current	See Terminal Limits	-1mA to +1mA
Zero Offset	½LSB, Max	•
TERMINAL LIMITS	±5mA	-10V to +1.5V
IMPEDANCE	0.3 ohm, Max	1.5k ohm, ±1%
FULL-SCALE CALIBRATION	10V -LSB, ±0.05%	2mA, ±2%
ACCURACY	±½LSB	±½LSB Rel. to F.S.
LINEARITY	±½LSB (±0.05% of Full Scale)	•
SETTLING TIME		
To 0.05% of F.S.	5μsec for 10V Step	300nsec for 2mA Step
OUTPUT CIRCUIT PROTECTION	Can be Opened or Shorted Indefinitely to Ground or ± Supply Voltage Without Damage.	Can be Opened or Shorted Indefinitely to Ground Without Damage.
POWER REQUIREMENT	±15VDC, ±2% @ ±15mA	•
POWER SUPPLY SENSITIVITY		
UNIPOLAR		
Zero	3ppm of F.S./%ΔV_S	•
Gain	150ppm of Reading/%ΔV_S	•
BIPOLAR		
Zero	10ppm of F.S./%ΔV_S	200ppm of F.S./%ΔV_S
Gain	300ppm of Reading/%ΔV_S	•
TEMPERATURE RANGE		
OPERATING	0 to +70°C	•
STORAGE	-55°C to +125°C	•
TEMPERATURE COEFFICIENT		
UNIPOLAR		
Zero	10ppm of F.S./°C	5ppm of F.S./°C
Gain	30ppm of Reading/°C	•
BIPOLAR		
Zero	30ppm of F.S./°C	•
Gain	30ppm of Reading Ref. to +F.S./°C	40ppm of Reading Ref. to -F.S./°C
PRICE		
(1-9)	$49.	•
(10-24)	$34.	•
(25-99)	$29.	•
(100+)	$27.	•

[1]Maximum V input +15V allowable.
•Specifications same as model DAC-10Z.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

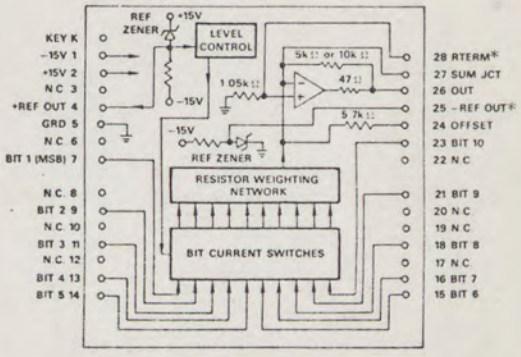
Dimensions shown in inches and (mm).



NOTE:

Terminal pins installed only in shaded hole locations.
See table below for deleted pins.
Module weight: 2 ounces (57 grams).
All pins are gold plated half-hard brass (MIL-G-45 204), 0.019" ±0.001" (0.48 ±0.03) dia.
For mounting card, order AC4102 @ $15.00.

BLOCK DIAGRAM
DAC-10Z & MDA-10Z



PINS SHOWN AS HAVING NO CONNECTIONS (N.C.) ARE DELETED. THE OUTPUT OP AMP ONLY APPEARS IN THE DAC-10Z's.

*NOTE: NOT ALL OF THE PINS SHOWN WITH CONNECTIONS TO THEM APPEAR ON EACH MODEL. THE PINS DELETED ON EACH MODEL ARE SHOWN BELOW:

MODEL	DELETED PINS
DAC-10Z-1	PINS 25, 28
DAC-10Z-3	PIN 28
MDA-10Z-25	PIN 25
MDA-10Z-110	NONE

ORDERING GUIDE:

AC-10Z-1	10-bit binary with amplifier, 0V to -10V output voltage.
AC-10Z-3	10-bit binary with amplifier, 10V to -10V output voltage.
DA-10Z-25	10-bit binary without amplifier, with 0mA to +2mA output current and 5kΩ nominal (4.85kΩ ±1%) gain resistor.
DA-10Z-110	10-bit binary without amplifier, -1mA to +1mA output current and 10kΩ nominal (9.70kΩ ±1%) gain resistor.

APPENDIX 2

PAPER TAPE LOADER

				LOAD 8	
000		LXI	B, 100	001	INCOMING
1				100	← PROGRAM
2				000	ADDRESS
3	LI:	IN	050	333	
4				050	
5		RRC		017	
6		JC	LI	332	
7				003	
010				000	
1		IN	051	333	
2				051	
3		STAX	B	002	
4		INX	B	003	
5		JMP	LI	303	
6				003	
7				000	

```
000-100: 061, 077, 000, 315, 031, 002, 001, 261,
000-110: 002, 021, 266, 002, 315, 011, 002, 315,
000-120: 031, 002, 076, 012, 315, 131, 002, 076,
000-130: 077, 315, 131, 002, 315, 111, 002, 315,
000-140: 131, 002, 365, 315, 031, 002, 361, 376,
000-150: 114, 312, 220, 000, 376, 104, 312, 300,
000-160: 000, 376, 107, 312, 301, 001, 376, 124,
000-170: 312, 371, 001, 376, 120, 312, 321, 001,
000-200: 001, 267, 002, 021, 321, 002, 315, 011,
000-210: 002, 303, 127, 000, 000, 000, 000, 000,
000-220: 315, 051, 002, 315, 021, 001, 102, 113,
000-230: 171, 346, 007, 000, 302, 257, 000, 120,
000-240: 131, 315, 150, 002, 000, 000, 000, 000,
000-250: 000, 000, 000, 200, 000, 000, 000, 315,
000-260: 040, 001, 174, 002, 003, 303, 230, 000,
000-270: 000, 000, 000, 200, 000, 000, 000, 000,
000-300: 315, 051, 002, 315, 021, 001, 102, 153,
000-310: 315, 071, 002, 315, 021, 001, 140, 102,
000-320: 113, 003, 076, 012, 315, 131, 002, 175,
000-330: 346, 007, 302, 345, 000, 124, 135, 315,
000-340: 031, 002, 315, 150, 002, 126, 315, 241,
000-350: 001, 076, 054, 315, 131, 002, 076, 040,
000-360: 315, 131, 002, 000, 000, 000, 000, 000,
000-370: 000, 000, 043, 175, 271, 302, 327, 000,
001-000: 174, 270, 302, 327, 000, 303, 100, 000,
001-010: 000, 000, 000, 000, 000, 000, 000, 000,
001-020: 000, 315, 040, 001, 134, 315, 040, 001,
001-030: 124, 311, 000, 000, 000, 000, 000, 000,
001-040: 315, 121, 001, 346, 017, 017, 017, 147,
001-050: 315, 161, 001, 346, 017, 007, 007, 007,
001-060: 264, 147, 315, 161, 001, 346, 017, 264,
001-070: 147, 315, 111, 002, 376, 015, 315, 131,
001-100: 002, 302, 111, 001, 076, 012, 315, 131,
001-110: 002, 311, 000, 000, 000, 000, 000, 000,
001-120: 000, 315, 111, 002, 376, 064, 362, 135,
001-130: 001, 315, 131, 002, 311, 315, 221, 001,
001-140: 315, 031, 002, 076, 077, 315, 131, 002,
001-150: 361, 303, 040, 001, 000, 200, 000, 000,
001-160: 000, 315, 111, 002, 376, 070, 362, 175,
001-170: 001, 315, 131, 002, 311, 315, 221, 001,
001-200: 315, 031, 002, 076, 077, 315, 131, 002,
001-210: 361, 303, 040, 001, 000, 000, 000, 000,
001-220: 000, 305, 001, 322, 002, 021, 354, 002,
001-230: 315, 011, 002, 301, 311, 000, 000, 000,
001-240: 000, 172, 346, 300, 007, 007, 366, 060,
001-250: 315, 131, 002, 172, 346, 070, 017, 017,
001-260: 017, 366, 060, 315, 131, 002, 172, 346,
001-270: 007, 366, 060, 315, 131, 002, 311, 000,
001-300: 000, 315, 051, 002, 315, 021, 001, 142,
001-310: 153, 351, 000, 000, 000, 000, 200, 000,
001-320: 000, 315, 051, 002, 315, 021, 001, 325,
001-330: 315, 071, 002, 315, 021, 001, 023, 301,
001-340: 315, 201, 002, 012, 315, 131, 002, 003,
001-350: 171, 273, 302, 343, 001, 170, 272, 302,
001-360: 343, 001, 315, 201, 002, 303, 100, 000,
001-370: 000, 315, 051, 002, 315, 021, 001, 046,
002-000: 000, 315, 221, 002, 022, 023, 303, 001,
002-010: 002, 012, 315, 131, 002, 003, 171, 273,
002-020: 302, 011, 002, 170, 272, 302, 011, 002,
002-030: 311, 076, 215, 315, 131, 002, 076, 012,
002-040: 315, 131, 002, 311, 000, 000, 000, 000,
002-050: 000, 315, 031, 002, 076, 123, 315, 131,
002-060: 002, 076, 077, 315, 131, 002, 311, 000,
002-070: 000, 315, 031, 002, 076, 105, 315, 131,
002-100: 002, 076, 077, 315, 131, 002, 311, 000,
002-110: 000, 333, 050, 017, 332, 111, 002, 333,
002-120: 051, 376, 030, 312, 100, 000, 346, 177,
002-130: 311, 365, 333, 050, 007, 332, 132, 002,
002-140: 361, 323, 051, 311, 000, 000, 000, 000,
002-150: 315, 241, 001, 076, 055, 315, 131, 002,
002-160: 123, 315, 241, 001, 076, 072, 315, 131,
002-170: 002, 076, 040, 315, 131, 002, 311, 000,
002-200: 000, 046, 060, 056, 000, 076, 000, 315,
002-210: 131, 002, 054, 175, 274, 302, 205, 002,
002-220: 311, 333, 050, 017, 332, 221, 002, 333,
002-230: 051, 376, 000, 302, 246, 002, 174, 376,
002-240: 001, 302, 221, 002, 076, 000, 046, 001,
002-250: 311, 040, 101, 104, 104, 122, 105, 123,
002-260: 123, 322, 305, 101, 104, 131, 240, 311,
002-270: 116, 126, 101, 314, 311, 104, 240, 303,
002-300: 317, 115, 115, 101, 116, 104, 254, 240,
002-310: 324, 322, 131, 240, 101, 107, 101, 311,
002-320: 116, 240, 311, 116, 126, 101, 314, 311,
002-330: 076, 000, 062, 070, 004, 076, 010, 062,
002-340: 071, 004, 000, 000, 000, 000, 000, 000,
002-350: 001,
READY
```

?

SYSTEM MONITOR
OCTAL LISTING

APPENDIX 3

PROCEDURAL OUTLINE FOR TIME AVERAGING/SINGLE SCAN STORAGE

Computer:

1) Turn on; press stop and reset simultaneously, releasing the reset button first. MEMR, M1, WO, and WAIT LED's should be lit; if not, reinitialize. If PROT LED is lit, throw the unprotect switch.
2) Load the papertape loader program through the switch register of the Altair. Set Altair to run; TTY to LINE.
3) Load the monitor; make sure to carefully align the first word of data on the paper tape (061_8) with the reader prongs on the Teletype. Set reader to START.
4) After the system monitor has been read into the Altair check location 100_8 to see if the first word of the monitor has entered this location. If not, check subsequent locations of memory against the paper tape. If memory two or three locations away begins to indicate that the program has partially entered, one can try loading those first few missing words onto the data switches and then running the monitor from loc. 100_8. If the program did not enter at all, or is displaced one or two memory locations, then you must reload the monitor. Check first to see if the paper tape loader is still in computer memory. Once the correct first word has entered loc. 100_8, the monitor should be run from location 100_8.
5) READY ? will appear at the TTY. For appropriate responses see monitor instructions.

6) Connect the interface modules as illustrated in Fig. 3-1. Make sure all grounds are continuous.

Prepare sample in usual manner; run spectrum. If you can obtain a spectrum set, the gain of the amplifier module should be set relatively low (see Table 2-1); if no spectrum can be obtained then the initial setting of the amp. should be relatively high.

ALLOW 15 MINUTE WARM-UP

7) Apply power to the interface by turning the power switch of the power supply to ON. Attach an oscilloscope set for low speed scan to the TEST POINT jack on the amplifier module. Set the microtoggle to TP. Attach signal inputs of amp. to SIGNAL OUTPUT jacks on the rear panel of the NMR. Place NMR into 7.5 second repetitive scan mode by pressing SET and CRO. Changing vertical deflection should appear on the ocs. screen - if signal is locked at ± 25v. reduce amp. gain and change offset adjust via the procedure outlined on p 187. Proper gain adjustment is base line of noise/signal at 0.0 V, and the highest positive going signal to touch the 10.0V line.

8) Spectrum should now be swept (either ~~or~~ externally or internally by the NMR's sweep circuits) at the normal 150 second scan rate. The amplifier gain will have to be increased to get the proper gain adjustment. (the offset may or may not have to be adjusted).

9) Place the microtoggle in the ADC position. Data acquisition can now begin; type G on the TTY, and input current starting address of the acquisition routine. INPUT NUMBER OF RAMPS - IN OCTAL PLEASE? will appear at the TTY.

(The data acquisition routine has been assumed to already be in computer memory.)

The computer request must be followed with the number of desired ramps: this number must be written in octal, and must be a power of 2 from 2^0 to 2^8. For single storage 000_8 may be typed - this will generate a single scan. After desired number of ramps have been entered on the TTY, (CR) is pressed, and the computer will be waiting for the first clock pulse informing it that data is available. Throwing the RELEASE/INITIALIZE switch to the RELEASE position will cause data acquisition to begin.

10) To stop the data acquisition process for the purpose of re-tuning the NMR or to readjust the amp. offset and gain (which may be necessary over long time averaging runs) press any TTY key. The current ramp will finish, and then the System will wait until another TTY key is pressed. In the interim, re-tuning, etc. may be done.